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Datasheet

InnoLux

G070ACE-LH3

CH-01-072

- Tentative Specification
- Preliminary Specification
- Approval Specification

MODEL NO.: G070ACE
SUFFIX: LH3

Customer:	
APPROVED BY	SIGNATURE
Name / Title _____	_____
Note	

Please return 1 copy for your confirmation with your signature and comments.	

Approved By	Checked By	Prepared By
陳立錚	林秋森	潘方傑

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

G070ACE-LH3 is a 7" TFT Liquid Crystal Display module with WLED Backlight unit and 30 pins 1ch-LVDS interface. This module supports 800xRGBx480 AAS mode and can display 262k or 16.7M colors.

The PSWG is to establish a set of displays with standard mechanical dimensions and select electrical interface requirements for an industry standard 7" WVGA LCD panel and the LED driving device for Backlight is built in PCBA.

1.2 FEATURE

- WVGA (800 x 480 pixels) resolution
- DE (Data Enable) only mode
- LVDS Interface with 1pixel/clock
- PSWG (Panel Standardization Working Group)
- Wide operating temperature.
- RoHS compliance

1.3 APPLICATION

- TFT LCD Monitor
- Factory Application
- Amusement

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	152.4 (H) x 91.44 (V) (7" diagonal)	mm	(1)
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	800 x R.G.B. x 480	pixel	-
Pixel Pitch	0.1905 (H) x 0.1905 (V)	mm	-
Pixel Arrangement	RGB vertical Stripe	-	-
Display Colors	16.7M / 262K	color	-
Display Mode	Normally Black	-	-
Surface Treatment	Hard Coating (3H), Anti-Glare	-	-
Module Power Consumption	Total 2.55 W @ cell 0.45 W, BL 2.1 W	W	Typ.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	164.5	165	165.5	mm	(1)
	Vertical (V)	103.5	104	104.5	mm	
	Thickness (T)	8.13	8.63	9.13	mm	
Bezel Area	Horizontal	154.3	154.60	154.9	mm	
	Vertical	93.34	93.64	93.94	mm	
Active Area	Horizontal	-	152.4	-	mm	
	Vertical	-	91.44	-	mm	
Weight			152		g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

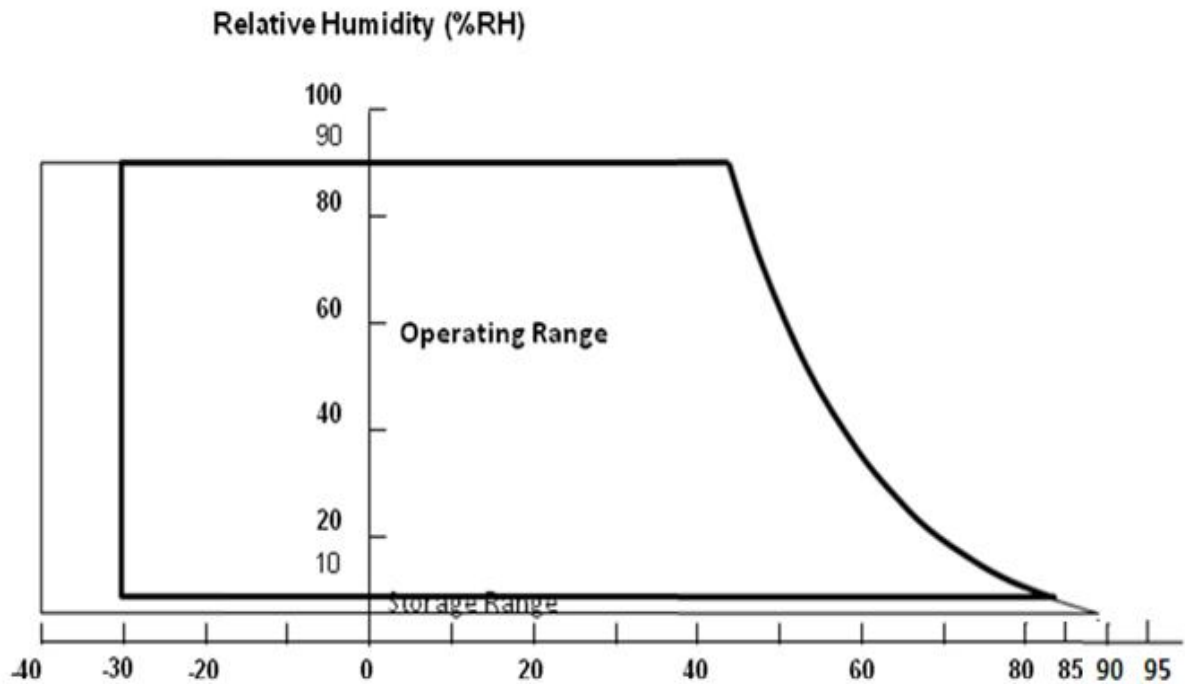
2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	Tst	-40	90	°C	(1)(2)
Operating Ambient Temperature	Top	-30	85	°C	

Note (1)

- (a) 90 %RH Max.
- (b) Wet-bulb temperature should be 39 °C Max.
- (c) No condensation.

Note (2) Panel surface temperature should be 0°C min. and 65°C max under Vcc=5.0V, fr =60Hz, typical LED string current, 25°C ambient temperature, and no humidity control . Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 85°C.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	3.6	V	(1)
Logic Input Voltage	V _{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Converter Voltage	V _i	0	18.0	V	(1), (2)
Enable Voltage	EN	---	7	V	
Backlight Adjust	Dimming	---	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to 3.2 for further information).

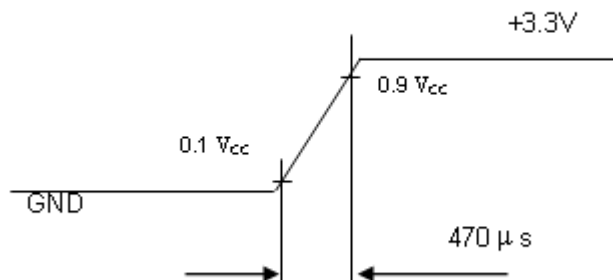
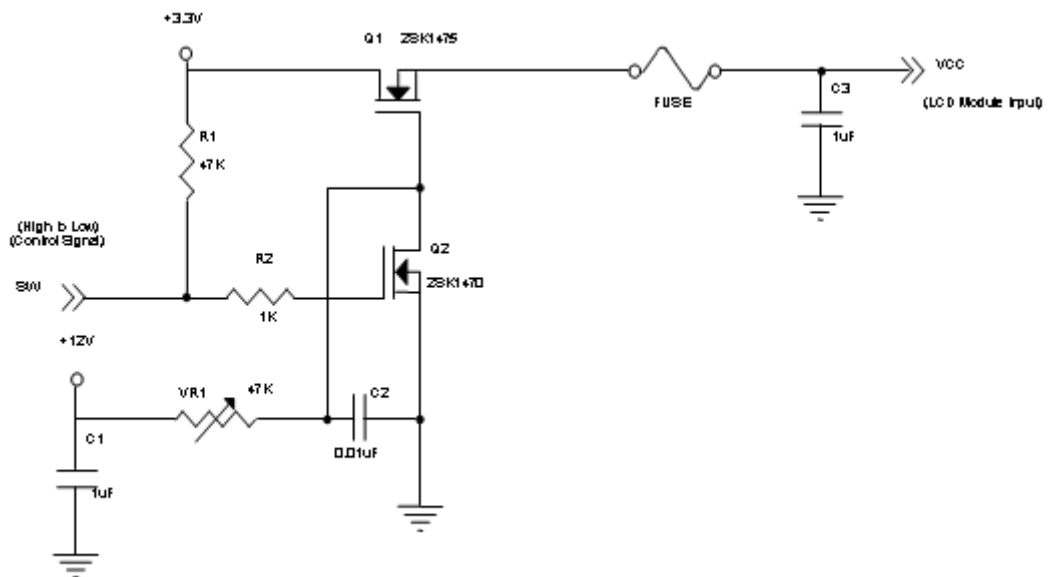
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V _{CC}	3.0	3.3	3.6	V	-
Ripple Voltage	V _{RP}	-	-	100	mVp-p	-
Rush Current	I _{RUSH}	-	-	2	A	(2)
Power Supply Current	White	-	135	200	mA	(3)a
	Black	-	85	135	mA	(3)b
LVDS differential input voltage	V _{id}	200	-	600	mV	
LVDS common input voltage	V _{ic}	1.0	1.2	1.4	V	
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	V _{TH}	-	+100	mV	-
	"L" Level	V _{TL}	-100	-	mV	-
Logic Input Voltage	"H" Level	V _{IH}	2.6	V _{CC}	V	
	"L" Level	V _{IL}	0	0.7	V	
Terminating Resistor	R _T	-	100	-	Ohm	-

Note (1)The module should be always operated within above ranges.

Note (2)Measurement Conditions:



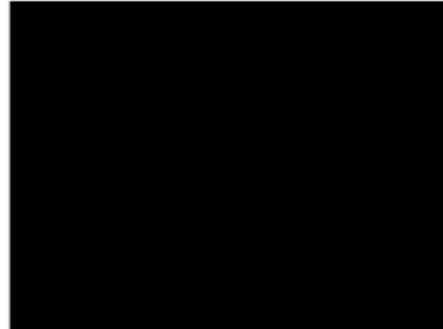
Note (3) The specified power supply current is under the conditions at $V_{CC} = 3.3V$, $T_a = 25 \pm 2^\circ C$, DC Current and $f_v = 60$ Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

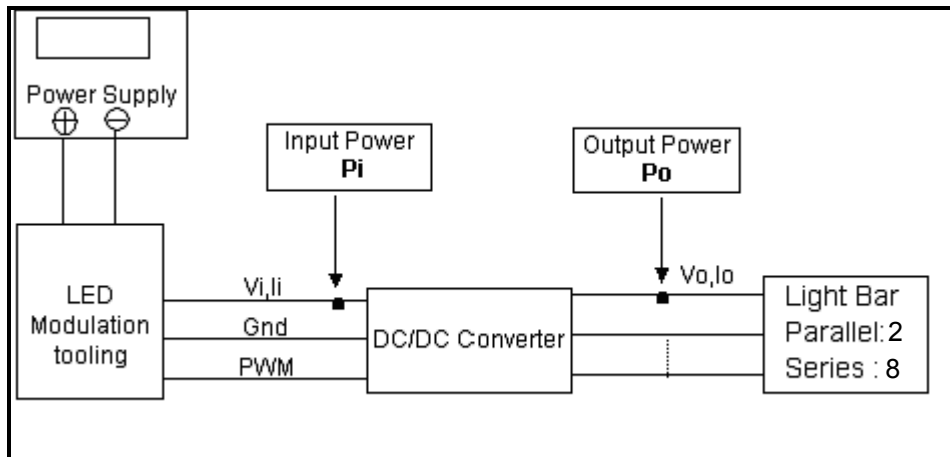


Active Area

3.2 BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Converter Power Supply Voltage	LED_Vin	10.8	12.0	13.2	V		
Converter Input Ripple Voltage	V _{IRP}	-	-	500	mV		
Converter Power Supply Current	I _i	0.15	0.17	0.2	A	@LED_Vin= 12V Duty=100%	
Converter Input Rush Current	I _{irsh}			3	A	@LED_Vin rising = 1mS(Vi=12V)	
Input Power Consumption	P _i	-	2.1	2.5	W	(1)	
EN Control Level	Backlight on	ENLED	2.0	3.3	5.0	V	
	Backlight off	(BLON)	0	-	0.3	V	
PWM Control Level	PWM High Level	Dimming	2.0	--	5.0	V	
	PWM Low Level	(E_PWM)	0	--	0.15	V	
PWN Noise Range	V _{Noise}	-	-	0.1	V		
PWM Control Frequency	f _{PWM}	190	200	20K	Hz	(3)	
PWM Dimming Control Duty Ratio	-		5	-	100	%	(3), @ 190Hz < f _{PWM} < 1kHz
			20	-	100	%	(3), @ 1kHz ≤ f _{PWM} < 20kHz
LED Life Time	L _{LED}	50,000		-	Hrs	(2)	

Note (1) LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) The lifetime of LED is estimated data and defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2 \text{ }^\circ\text{C}$ and Duty 100% until the brightness becomes $\leq 50\%$ of its original value. Operating LED at high temperature condition will reduce life time and lead to color shift.

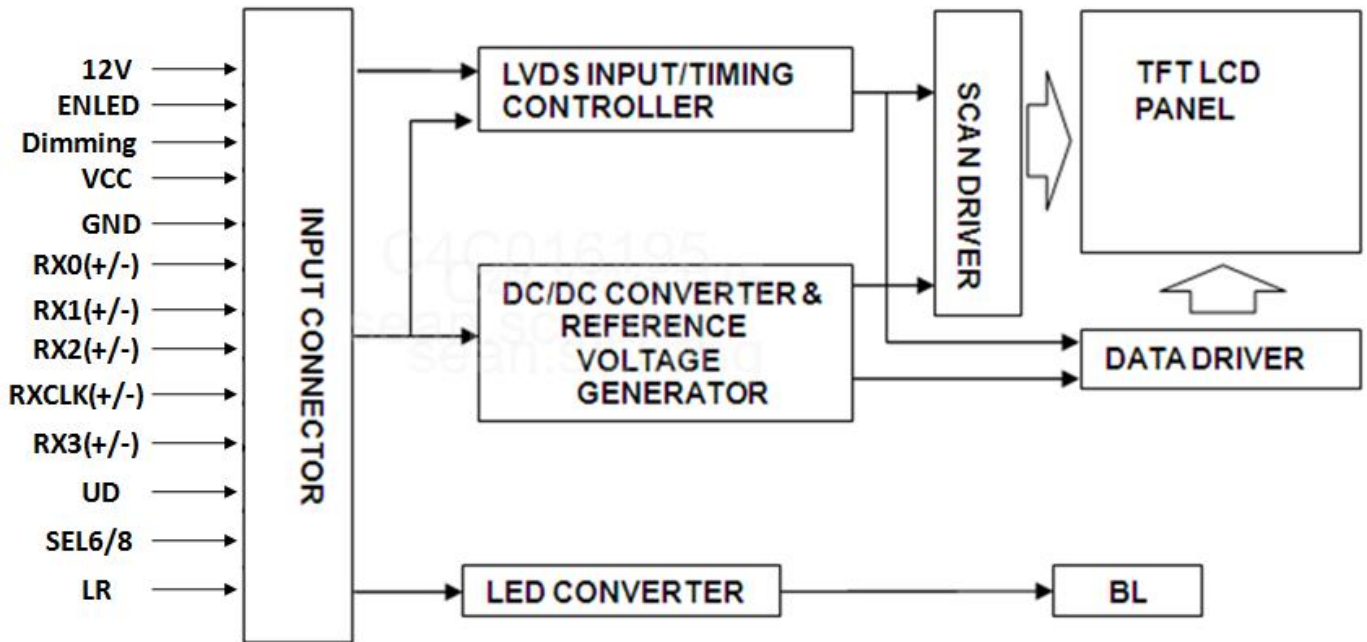
Note (3) At 190 ~1kHz PWM control frequency, duty ratio range is restricted from 5% to 100%.

1K ~20kHz PWM control frequency, duty ratio range is restricted from 20% to 100%.

If PWM control frequency is applied in the range from 1KHz to 20KHZ, The “non-linear” phenomenon on the Backlight Unit may be found. So It’ s a **suggestion** that PWM control frequency should be **less than 1KHz**.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin No.	Symbol	Function	Polarity	Note
1	12V	LED power		-
2	12V	LED power		-
3	12V	LED power		-
4	12V	LED power		-
5	ENLED	Enable pin		-
6	Dimming	Backlight Adjust		-
7	NC	No Connction (Reserve for INX test)		(4)
8	NC	No Connction (Reserve for INX test)		(4)
9	VCC	Power supply: +3.3V		-
10	VCC	Power supply: +3.3V		-
11	GND	Ground		-
12	GND	Ground		-
13	RX0-	Negative transmission data of pixel 0	Negative	-
14	RX0+	Positive transmission data of pixel 0	Positive	-
15	GND	Ground		-
16	RX1-	Negative transmission data of pixel 1	Negative	-
17	RX1+	Positive transmission data of pixel 1	Positive	-
18	GND	Ground		-
19	RX2-	Negative transmission data of pixel 2	Negative	-
20	RX2+	Positive transmission data of pixel 2	Positive	-
21	GND	Ground		-
22	RXCLK-	Negative of clock	Negative	-
23	RXCLK+	Positive of clock	Positive	-
24	GND	Ground		-
25	RX3-	Negative transmission data of pixel 3	Negative	-
26	RX3+	Positive transmission data of pixel 3	Positive	-
27	UD	Gate Driver Up/Down scan control. When UD=H, reverse scan When UD=L, normal scan		(3)
28	SEL6/8	LVDS 6/8 bit select function control, Low → 6 bit Input Mode High or NC → 8bit Input Mode		(3)
29	LR	Source Driver Right/ Left scan control. When LR=H, normal scan When LR=L, reverse scan		(3)
30	GND	Ground		

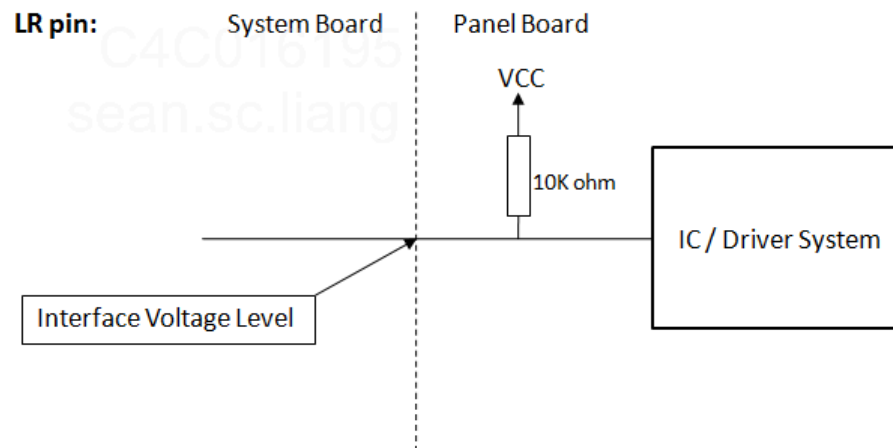
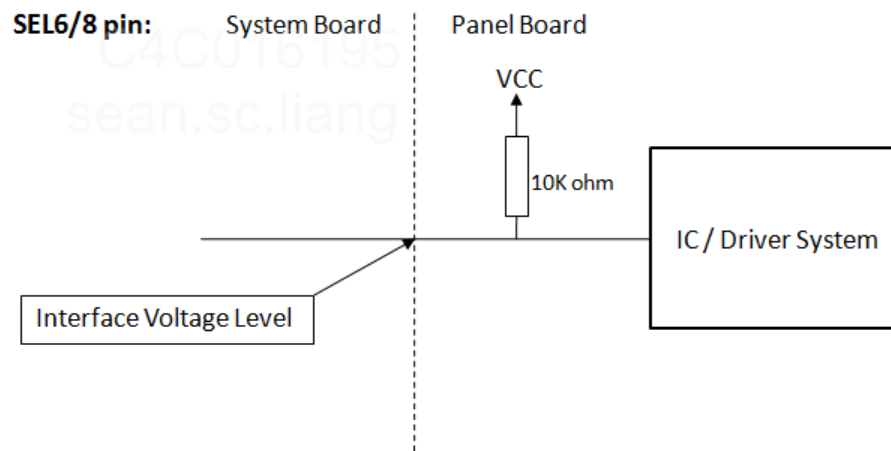
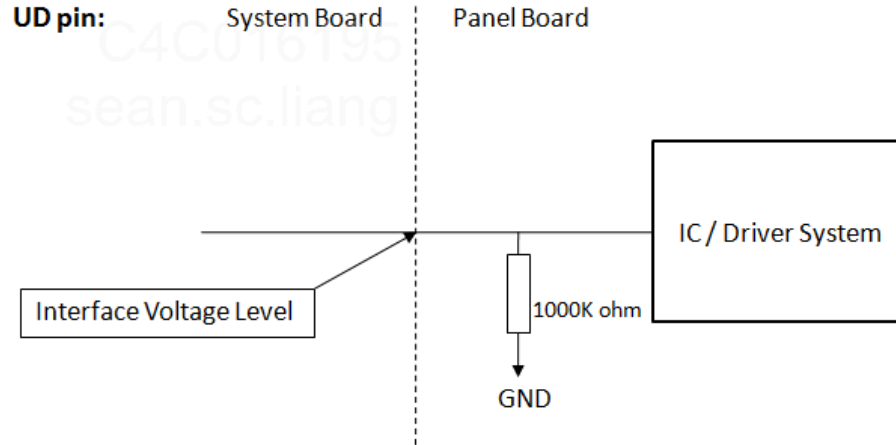
Note (1) Connector Part No.: Starconn 093G30-B0001A-G4.

Note (2) User's connector Part No:

Mating Wire Cable Connector Part No. :FI-X30H (JAE) or FI-X30HL (JAE)

Note (3) "Low" stands for 0V. "High" stands for 3.3V

Note (4) Pin7, Pin8 input signals should be set to no connection or ground, this module



5.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

Note (1)0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

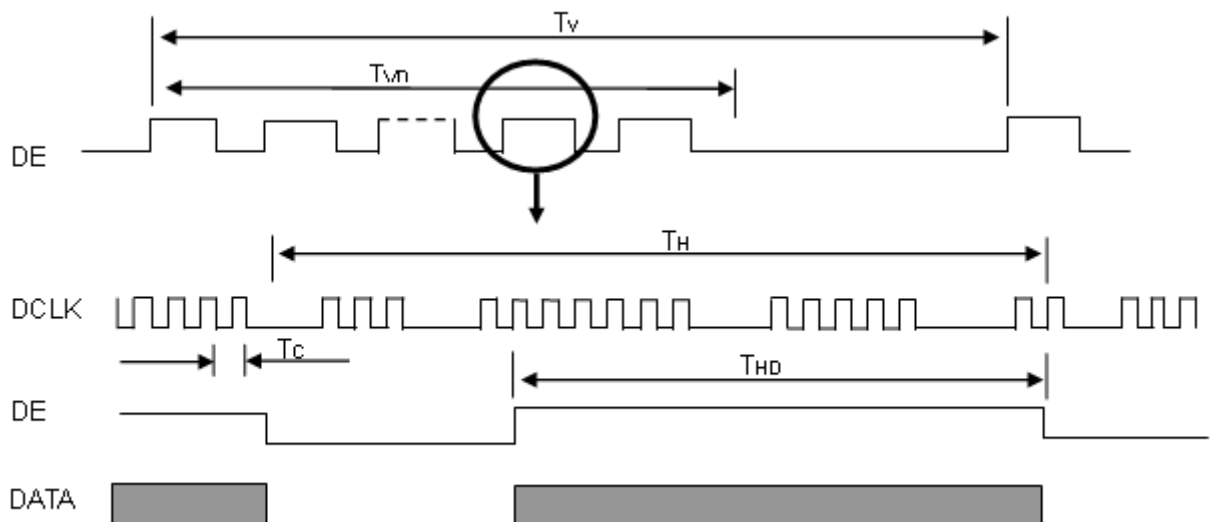
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F _c	25.2	25.4	35.7	MHz	-
	Period	T _c		39.37		ns	
	Input cycle to cycle jitter	T _{rcj}	-0.02*T _c	-	0.02*T _c	ns	(a)
	Input Clock to data skew	TLVCCS	-0.02*T _c	-	0.02*T _c	ps	(b)
	Spread spectrum modulation range	F _{clk_in_mod}	-	-	1.02*F _c	MHz	(c)
	Spread spectrum modulation frequency	F _{SSM}	23	-	93	KHz	
Vertical Display Term	Frame Rate	F _r	-	60	-	Hz	-
	Total	T _v	488	490	611	T _h	T _v =T _{vd} +T _{vb}
	Active Display	T _{vd}	480	480	480	T _h	-
	Blank	T _{vb}	8	10	131	T _h	-
Horizontal Display Term	Total	T _h	860	864	974	T _c	T _h =T _{hd} +T _{hb}
	Active Display	T _{hd}	800	800	800	T _c	-
	Blank	T _{hb}	60	64	174	T _c	-

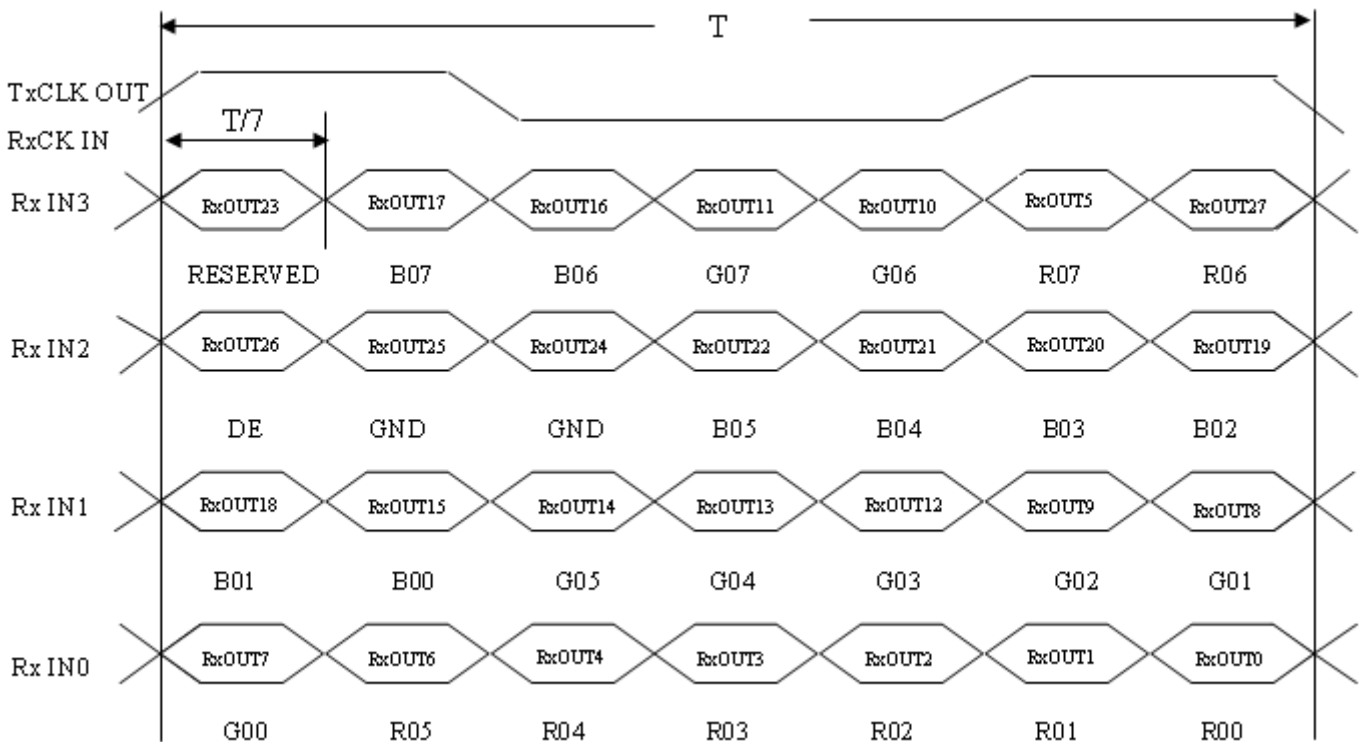
Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note (2) The Tv(Tvd+Tvb) must be integer, otherwise, the module would operate abnormally.

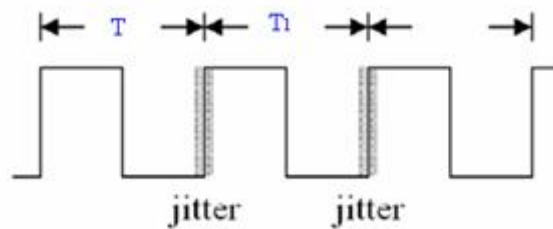
INPUT SIGNAL TIMING DIAGRAM



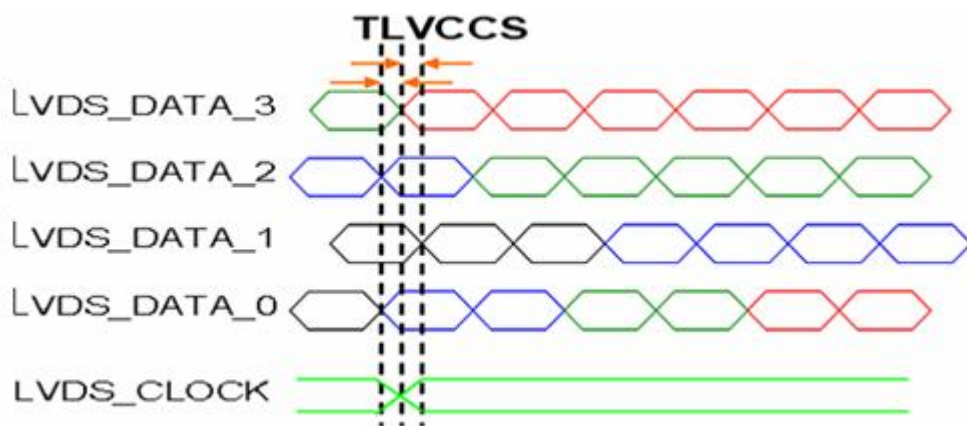
TIMING DIAGRAM of LVDS



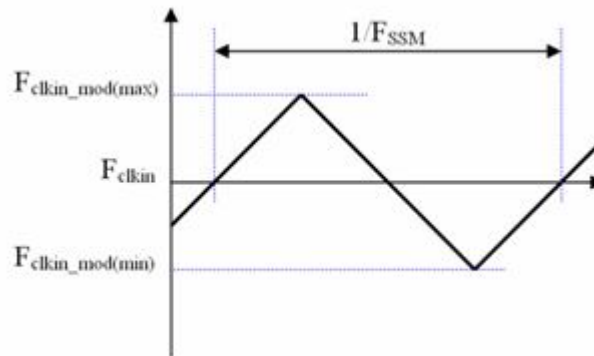
Note (a) The input clock cycle-to-cycle jitter is defined as below figures. $T_{rc1} = |T1 - T1|$



Note (b) Input Clock to data skew is defined as below figures.

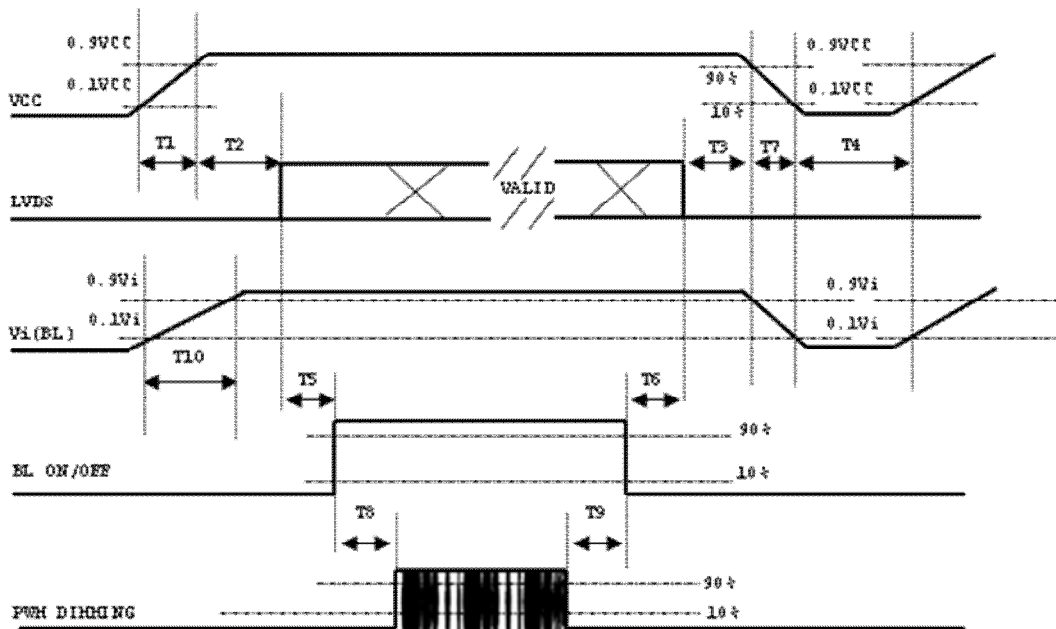


Note (c) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



Parameter	Value			Units Min
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	450	-	-	ms
T6	200	-	-	ms
T7	10	-	100	ms

T8	10	-	-	ms
T9	10	-	-	ms
T10	20	-	50	ms

Note

- (1)The supply voltage of the external system for the module input should be the same as the definition of Vcc.
- (2)When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.
- (3)In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.
- (4)T4 should be measured after the module has been fully discharged between power off and on period.
- (5)Interface signal shall not be kept at high impedance when the power is on.
- (6)INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.
- (7)There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec".

6.3 SCANNING DIRECTION

The following figures show the image see from the front view. The arrow indicates the direction of scan.

Fig.1 Normal Scan



PCBA on the bottom side

Fig.2 Reverse Scan



PCBA on the bottom side

Fig. 1 Normal scan (pin 27, UD = Low, pin 29 LR = High)

Fig. 2 Reverse scan (pin 27, UD = High, pin 29 LR = Low)

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value and tolerance in "ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown here and all items are measured at the center point of screen unless otherwise noted. The following items should be measured under the test conditions described above and stable conditions shown in Note (5).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Color Chromaticity	Red	Rx	Typ - 0.05	0.590	Typ + 0.05	-	(1), (5)	
		Ry		0.330				
	Green	Gx		0.334				
		Gy		0.600				
	Blue	Bx		0.150				
		By		0.054				
	White	Wx		0.313				
		Wy		0.329				
Center Luminance of White	LC	Grayscale Maximum	400	500		cd/m ²	(4), (5)	
Contrast Ratio	CR		600	800			(2), (5)	
Response Time	TR	$\theta X=0^\circ, \theta Y=0^\circ$	-	13	18	ms	(3)	
	TF		-	12	17			
White Variation	δW	$\theta X=0^\circ, \theta Y=0^\circ$	70	-	-	%	(5), (6)	
Viewing Angle	Horizontal	$\theta X+$	$CR \geq 10$	80	89	-	Deg.	(1), (5)
		$\theta X-$		80	89	-		
	Vertical	$\theta Y+$		80	89	-		
		$\theta Y-$		80	89	-		

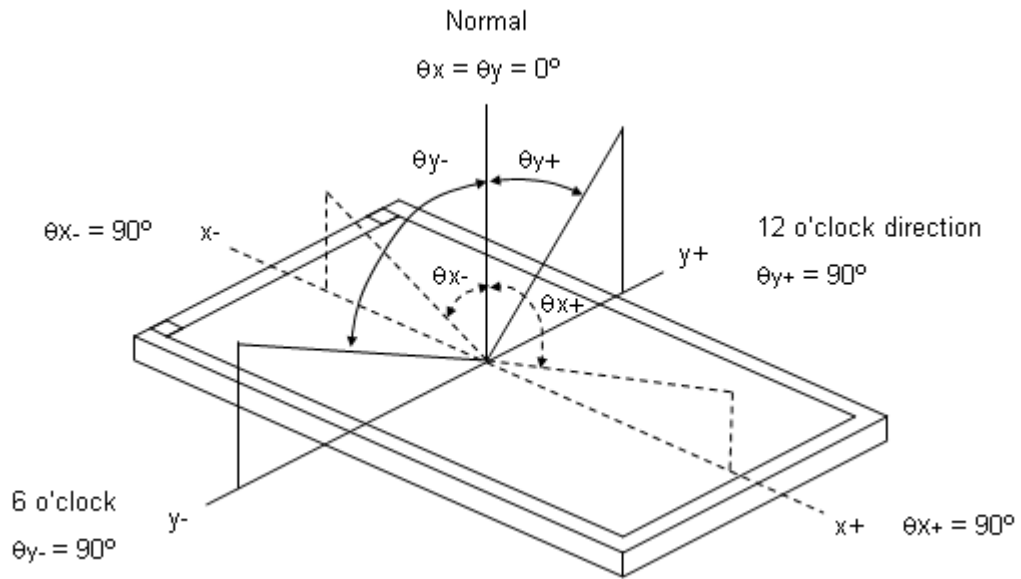
Definition :

Grayscale Maximum : Grayscale 255 (10 bits: grayscale 1023 ; 8 bits : grayscale 255 ; 6 bits: grayscale 63)

White : Luminance of Grayscale Maximum (All R,G,B)

Black : Luminance of grayscale 0 (All R,G,B)

Note (1) Definition of Viewing Angle (θ_x, θ_y):

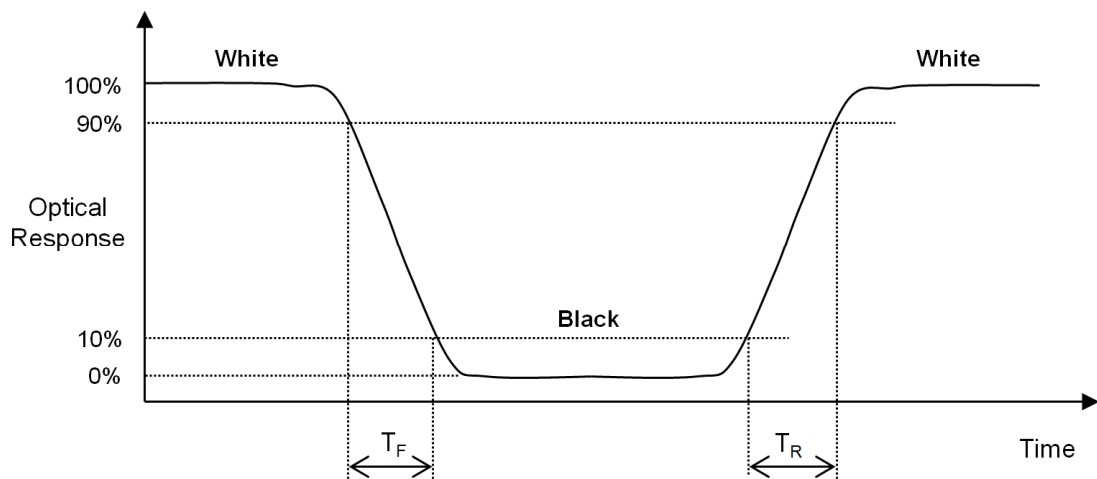


Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression at center point.

$$\text{Contrast Ratio (CR)} = \text{White} / \text{Black}$$

Note (3) Definition of Response Time (T_R, T_F):

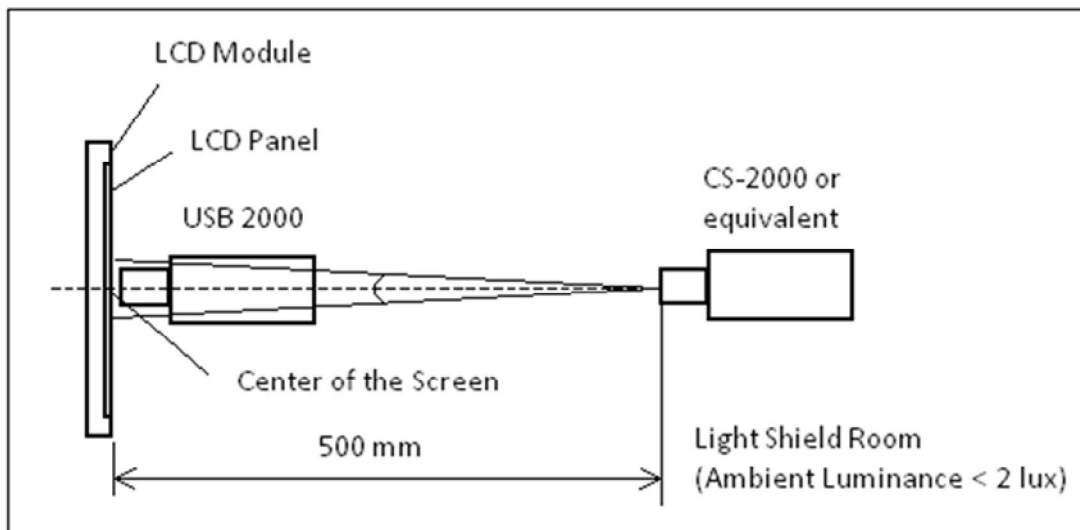


Note (4) Definition of Luminance of White (L_c):

Measure the luminance of White at center point.

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room. The measurement placement of module should be in accordance with module drawing.

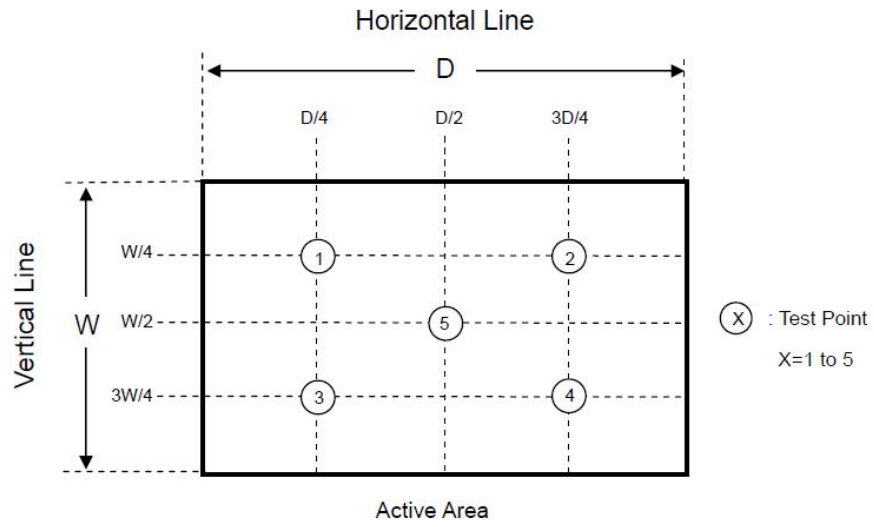


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points.

Luminance of White : $L(X)$, where X is from 1 to 5.

$$\delta W = \frac{\text{Minimum [} L(1) \text{ to } L(5) \text{]}}{\text{Maximum [} L(1) \text{ to } L(5) \text{]}} \times 100\%$$



8. RELIABILITY TEST CRITERIA

Test Item	Test Condition	Note
High Temperature Storage Test	90°C, 240 hours	(1),(2) (4),(5)
Low Temperature Storage Test	-40°C, 240 hours	
Thermal Shock Storage Test	-30°C, 0.5hour \longleftrightarrow 80°C, 0.5hour; 1hour/cycle,100cycles	
High Temperature Operation Test	85°C, 240 hours	
Low Temperature Operation Test	-30°C, 240 hours	
High Temperature & High Humidity Operation Test	60°C, RH 90%, 240 hours	
Shock (Non-Operating)	50G, 11ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$	(2), (3)
Vibration (Non-Operating)	1.5G, 10 ~ 300 Hz, 10min/cycle, 3 cycles each X, Y, Z	

Note (1) There should be no condensation on the surface of panel during test ,

Note (2) Temperature of panel display surface area should be 85°C Max.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (4) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

Note (5) Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 34 pcs LCD modules / 1 Box
- (2) Box dimensions: 465 (L) X 362 (W) X 314 (H) mm
- (3) Weight: approximately TBD Kg (34modules per box)

9.2 PACKING METHOD

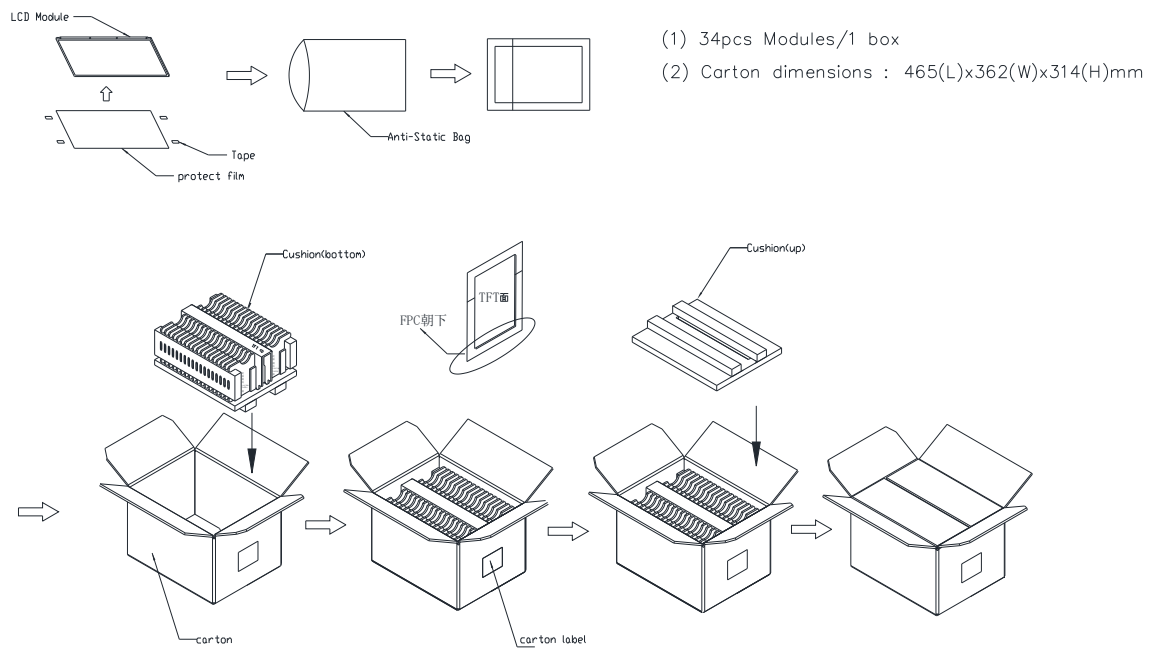
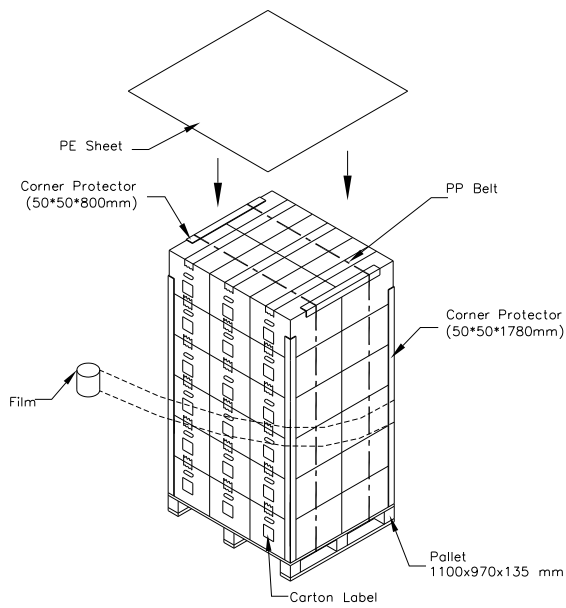


Figure. 9-1 Packing method

Sea / Land Transportation (40ft Container)



Air Transportation

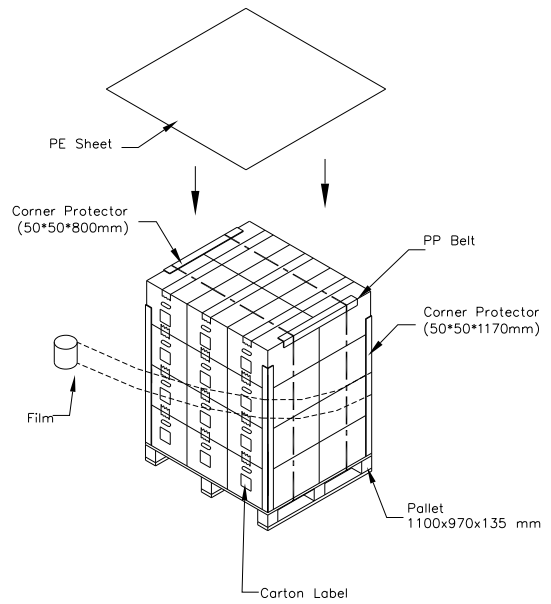


Figure. 9-2 Packing method

9.3 UN-PACKING METHOD

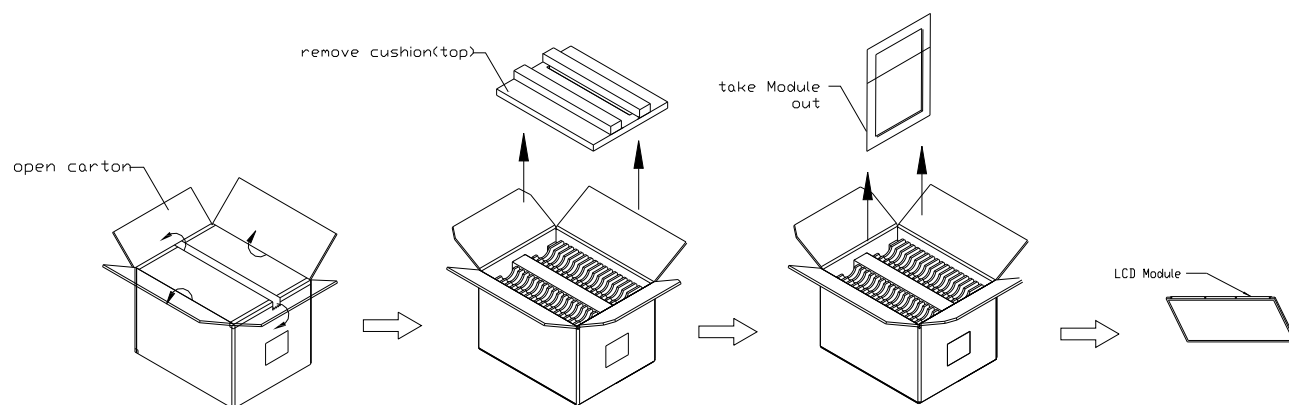
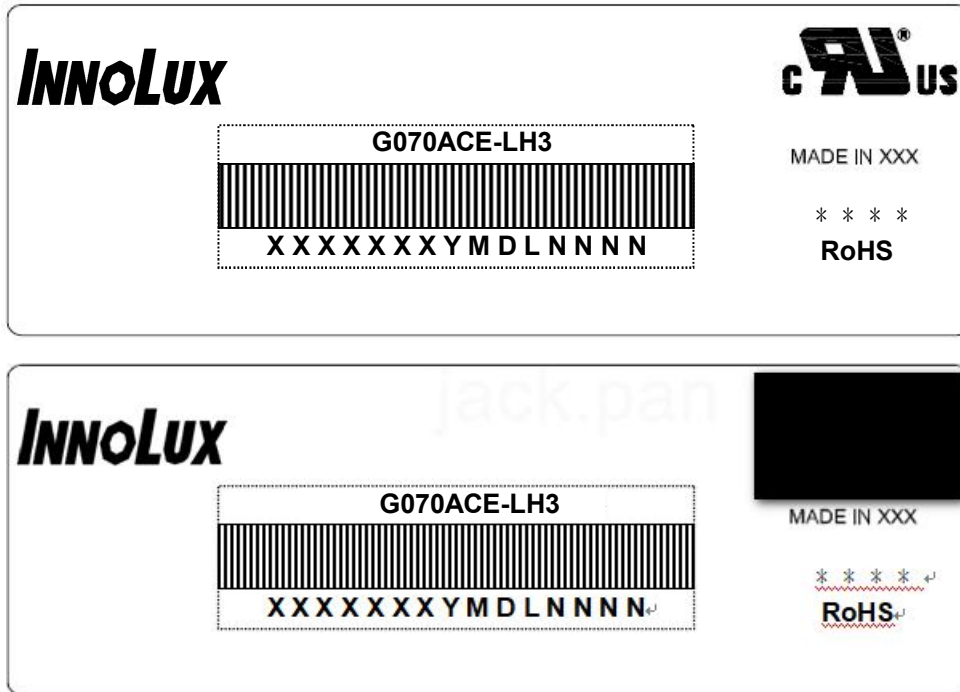


Figure. 9-3 UN-Packing method

10. DEFINITION OF LABELS

10.1 INX MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

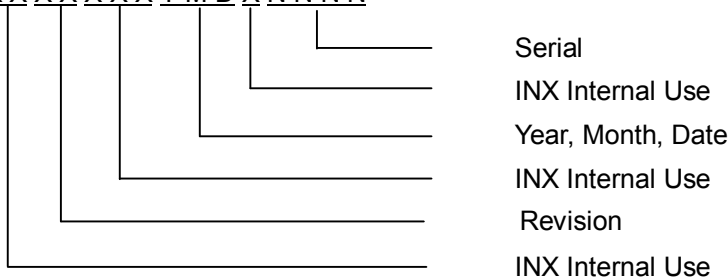


Note (1) Safety Compliance(UL logo) will open after C1 version.

(a) Model Name: G070ACE-LH3

(b) * * * * : Factory ID

(c) Serial ID: XXXXXXYMDXNNNN



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2021~2029
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

11. PRECAUTIONS**11.1 ASSEMBLY AND HANDLING PRECAUTIONS**

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.




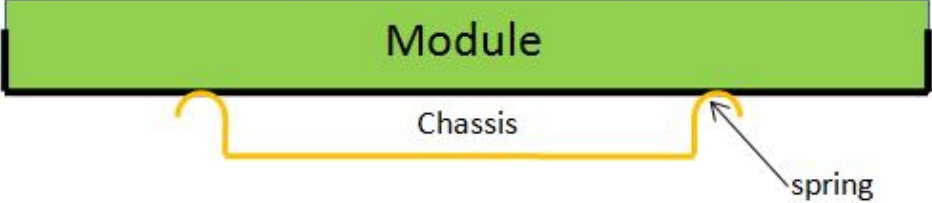
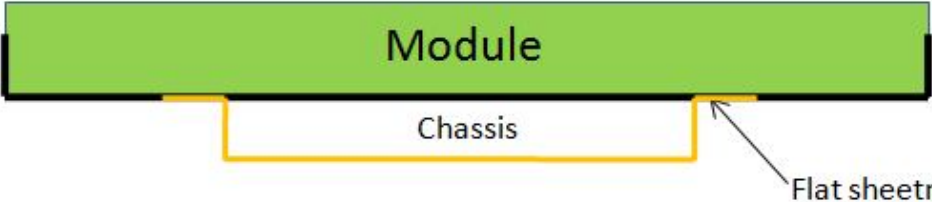
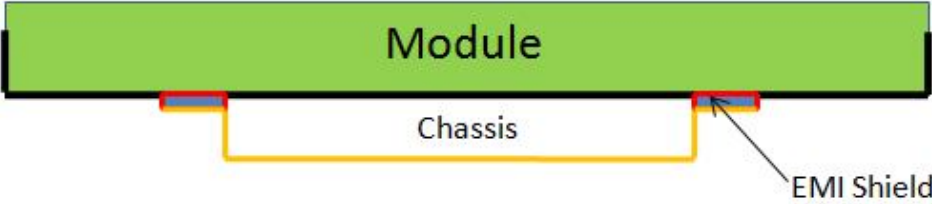
11.2 STORAGE PRECAUTIONS

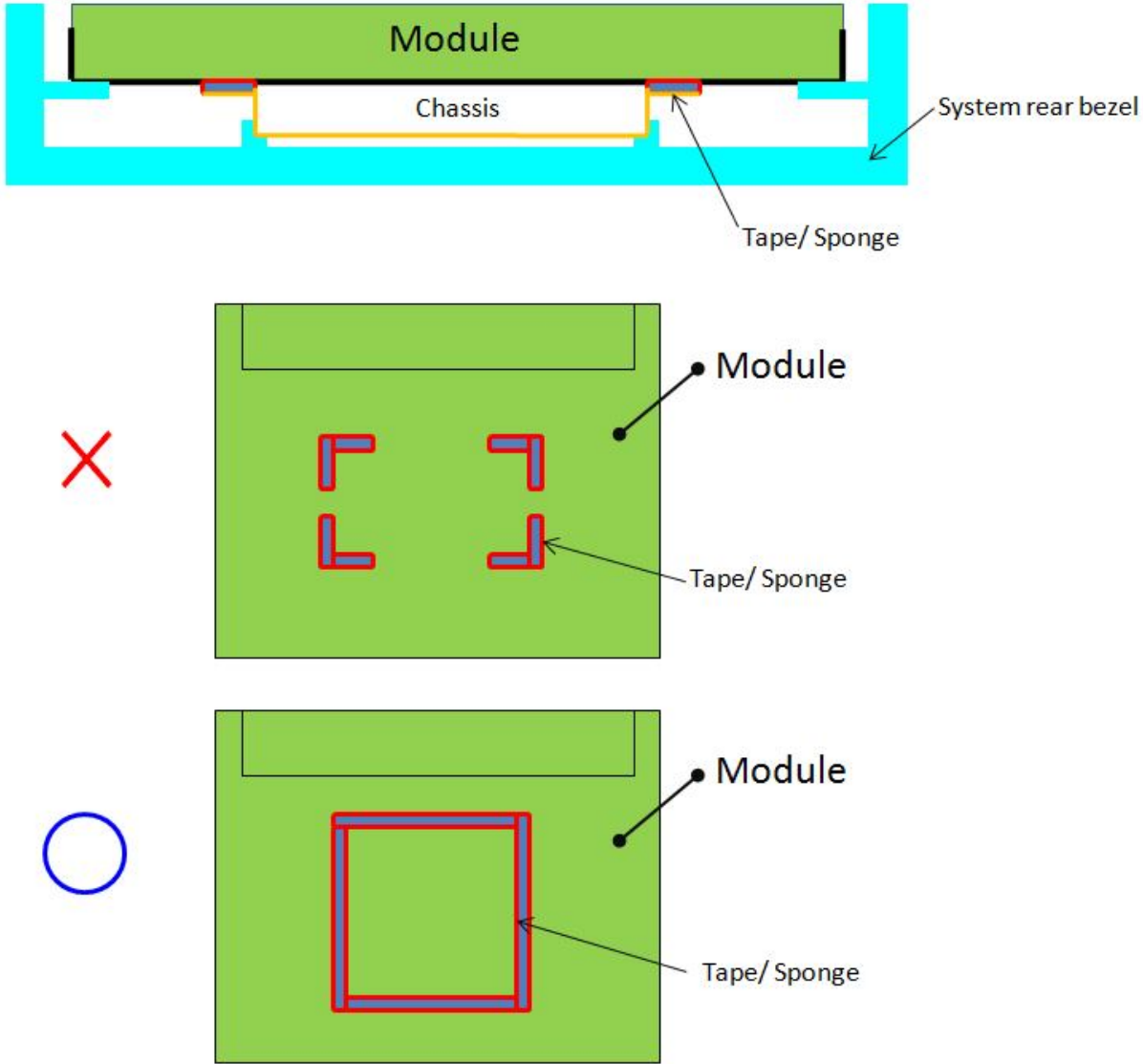
- (1)When storing for a long time, the following precautions are necessary.
 - (a) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 30°C at humidity 50+-10%RH.
 - (b) The polarizer surface should not come in contact with any other object.
 - (c) It is recommended that they be stored in the container in which they were shipped.
 - (d) Storage condition is guaranteed under packing conditions.
 - (e)The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition
- (2)High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (3)It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (4)It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

11.3 OTHER PRECAUTIONS

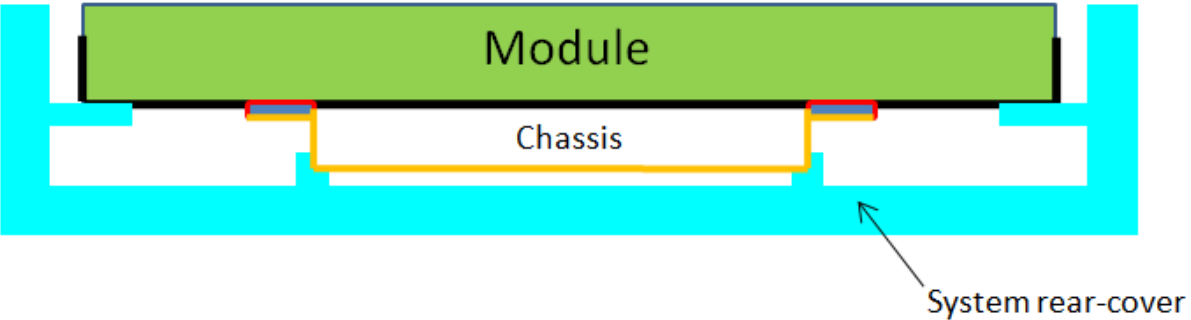
- (1) Normal operating condition
 - (a) Display pattern: dynamic pattern (Real display)
 - (Note) Long-term static display can cause image sticking.
- (2) Operating usages to protect against image sticking due to long-term static display
 - (a) Suitable operating time: under 16 hours a day.
 - (b) Static information display recommended to use with moving image.
 - (c) Cycling display between 5 minutes' information(static) display and 10 seconds' moving image.
- (3) Abnormal condition just means conditions except normal condition.

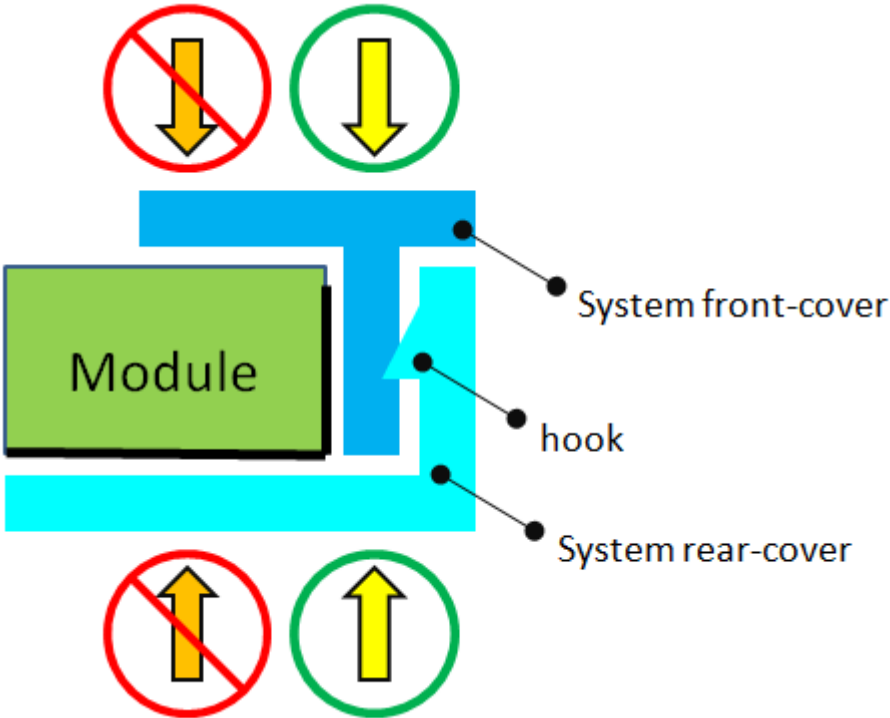
Appendix . SYSTEM COVER DESIGN NOTICE

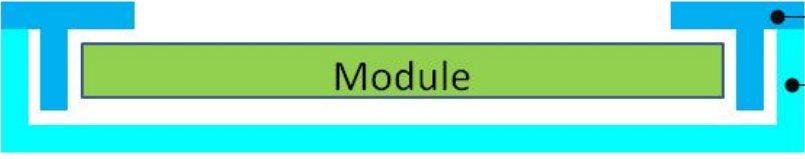
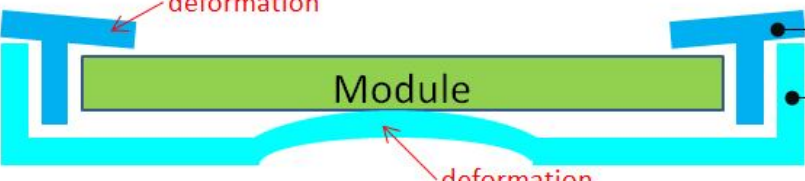
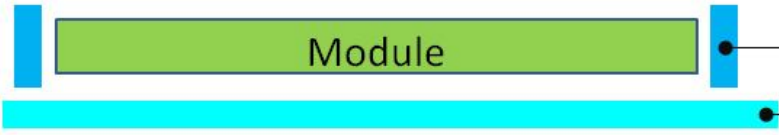
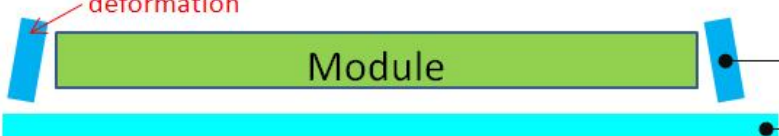
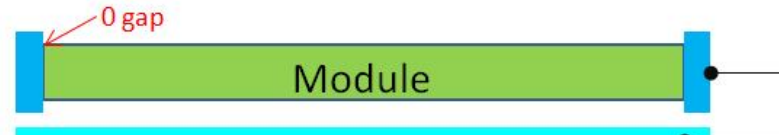
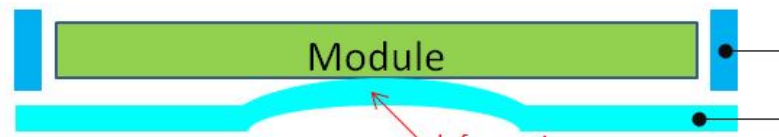
1	Set Chassis and IAVM Module touching Mode
  	  
Definition	<p>a. To prevent from abnormal display & white spot after mechanical test, it is not recommended to use spring type chassis.</p> <p>b. We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, second is Flat sheet metal type chassis.</p>

2	Tape/Sponge design on system inner surface
 <p>The top diagram shows a cross-section of a system with a green Module on a yellow Chassis, held in place by a cyan System rear bezel. Red Tape/Sponge is applied between the Module and Chassis. The middle diagram, marked with a red 'X', shows a top-down view of the Module with four separate L-shaped Tape/Sponge pieces at the corners. The bottom diagram, marked with a blue circle, shows a top-down view of the Module with a single rectangular Tape/Sponge piece covering the entire back surface.</p>	
Definition	<p>a. To prevent from abnormal display & white spot after mechanical test, we suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot.</p> <p>b. When using the Tape/Sponge, we suggest it be lay over between set chassis and Module rear cover. It is not recommended to add Tape/Sponge in separate location. Since each Tape/Sponge may act as pressure concentration location.</p>

3	System inner surface examination
<p>The diagram illustrates the system inner surface examination. The top part shows a green 'Module PCBA' with a red hatched area labeled 'The hatch area'. The bottom part shows a cross-section of the 'Module' (green) mounted on a 'System cover inner surface' (cyan). Labels include 'Burr', 'PCBA', 'Chassis', and 'Step'.</p>	
Definition	<p>a. The hatch area on Module PCBA should keep at least 1mm gap(X,Y,Z direction) to any structure with system cover inner surface.</p> <p>b. Burr, Step, PCB protrusion may cause stress concentration. White spot may occur during reliability test.</p>

4	Material used for system rear-cover
	
Definition	<p>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss position for module's bracket are deformed open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</p>

5	Assembly SOP examination for system front-cover with hook structure
	
Definition	<p>To prevent panel crack during system front-cover assembly process with hook structure, it is not recommended to press panel or any location that relate directly to the panel.</p>

6	Permanent deformation of system cover after reliability test
○	 <ul style="list-style-type: none"> ● System front-cover ● System rear-cover
✗	 <ul style="list-style-type: none"> ● System front-cover ● System rear-cover
○	 <ul style="list-style-type: none"> ● System front-cover ● System rear-cover
✗	 <ul style="list-style-type: none"> ● System front-cover ● System rear-cover
✗	 <ul style="list-style-type: none"> ● System front-cover ● System rear-cover
✗	 <ul style="list-style-type: none"> ● System front-cover ● System rear-cover
Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell crack.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

7	Design gap A between panel & any components on system rear-cover
Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

8	Design gap B between system front-cover & panel surface
Definition	<p>Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure.</p> <p>To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

9	Design gap C between panel & system front-cover or protrusions
Definition	<p>Gap between panel & system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.</p> <p>The gap should be large enough to absorb the maximum displacement during the test.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

10	Design distance between TP AA to LCD AA
Definition	TP VA should avoid TP ink area covering LCD AA or causing the module frame to be exposed.

11	Use OCR Lamination
<p>The diagram illustrates two methods of OCR lamination. The top diagram, marked with a red 'X', shows 'Line pooling' occurring at the edges of the 'TP or Cover Glass' layer. The bottom diagram, marked with a green circle, shows the correct method: 'OCR overflow' and 'Add Side glue' at the edges to prevent pooling. Labels include 'Display Area', 'TP or Cover Glass', and 'OCR'.</p>	
Definition	<ol style="list-style-type: none"> 1.OCR glue as possible beyond module, in order to avoid Line Pooling 2.Add side glue to avoid Line Pooling

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, the UK and the USA. For more information please contact:

Headquarters

Germany



FORTEC Elektronik AG

Augsburger Str. 2b
82110 Germering

Phone: +49 89 894450-0
E-Mail: info@fortecag.de
Internet: www.fortecag.de

Fortec Group Members

Austria



Distec GmbH Office Vienna

Nuschinggasse 12
1230 Wien

Phone: +43 1 8673492-0
E-Mail: info@distec.de
Internet: www.distec.de

Germany



Distec GmbH

Augsburger Str. 2b
82110 Germering

Phone: +49 89 894363-0
E-Mail: info@distec.de
Internet: www.distec.de

Switzerland



ALTRAC AG

Bahnhofstraße 3
5436 Würenlos

Phone: +41 44 7446111
E-Mail: info@altrac.ch
Internet: www.altrac.ch

United Kingdom



Display Technology Ltd.

Osprey House, 1 Osprey Court
Hichingbrooke Business Park
Huntingdon, Cambridgeshire, PE29 6FN

Phone: +44 1480 411600
E-Mail: info@displaytechnology.co.uk
Internet: www.displaytechnology.co.uk

USA



Apollo Display Technologies, Corp.

87 Raynor Avenue,
Unit 1 Ronkonkoma,
NY 11779

Phone: +1 631 5804360
E-Mail: info@apolloDisplays.com
Internet: www.apolloDisplays.com