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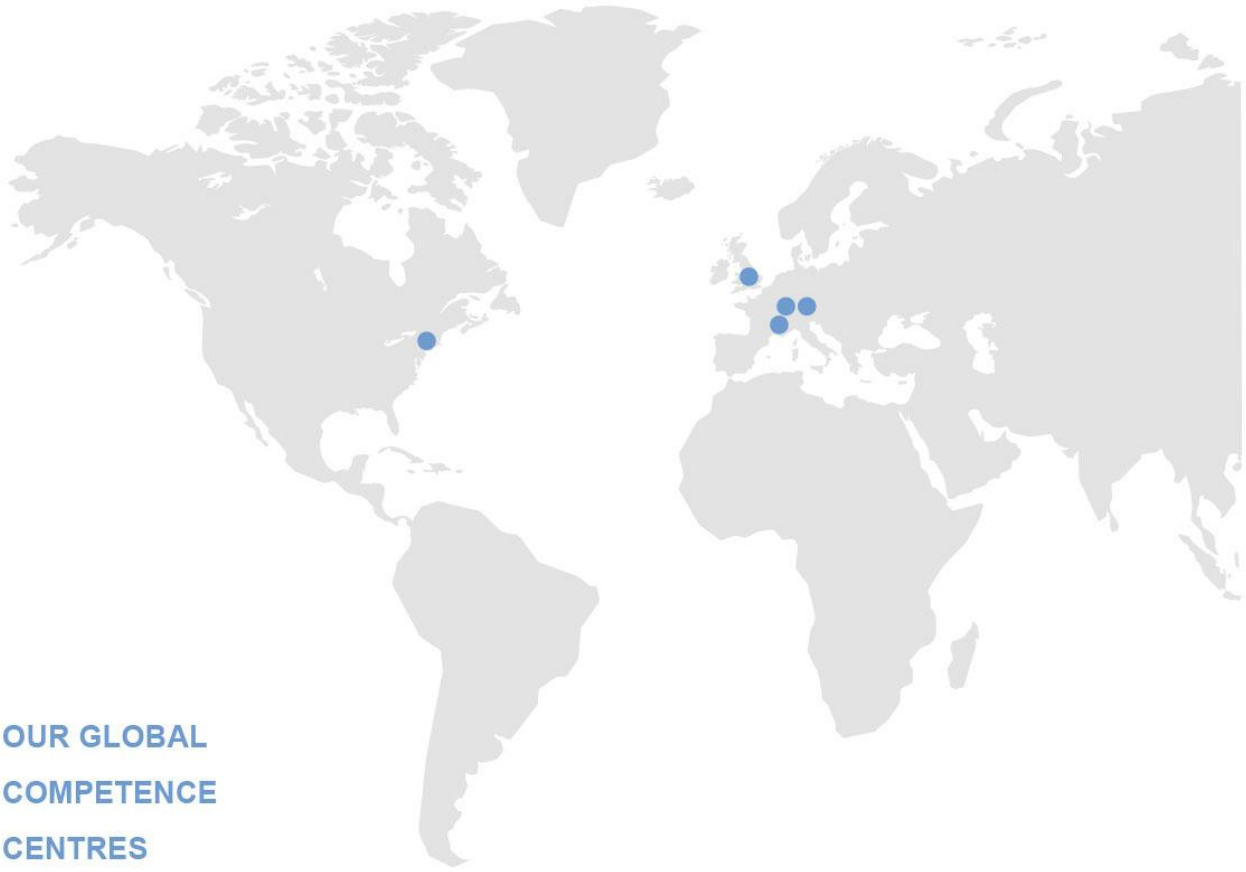

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DISPLAY TECHNOLOGY

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# Datasheet

# AUO

## G050TAN01.0

UP-02-176

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**( V ) Preliminary Specifications**
**( ) Final Specifications**

| | |
|---|---|
| **Module** | 5” Inch Color TFT-LCD |
| **Model Name** | G050TAN01.0 |

| **Customer** | **Date** | **Approved by** | **Date** |
|---|---|---|---|
| | | Grace Hung | 2017/11/22 |
| **Checked & Approved by** | | **Prepared by** | |
| | | Jon Tseng | 2017/11/22 |
| | | General Display Business Unit / AU Optronics corporation | |

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# Contents



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## Record of Revision

| Version and Date | Page | Old description | New Description |
|---|---|---|---|
| 0.0 Nov 22, 2017 | All | First draft specification | - |
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# 1. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any direction.
9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
15) The data on this specification sheet is applicable when LCD module is placed in landscape position.
16) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.

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# 2. General Description

This specification applies to the Color Active Matrix Liquid Crystal Display G050TAN01.0 composed of a TFT-LCD display, a driver and power supply circuit, and a LED backlight system. The screen format is intended to support HD (720(H) x 1280(V)) screen and 16.7M (8-bits).

All input signals are MIPI interface.

G050TAN01.0 designed with wide viewing angle; wide temperature and long life LED backlight is well suited for industial applications.

G050TAN01.0 is a RoHS product.

## 2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

| Items | Unit | Specifications |
|---|---|---|
| Screen Diagonal | [inch] | 4.99 |
| Active Area | [mm] | 62.1 x 110.4 |
| Pixels H x V | | 720 (RGB) x 1280 |
| Pixel Pitch | [mm] | 0.086 X 0.086 |
| Pixel Arrangement | | R.G.B. Vertical Stripe |
| Display Mode | | Normally Black |
| Nominal Input Voltage VDD | [Volt] | VDDI=1.8V, VCI=2.8V |
| Power Consumption | [Watt] | 1.65 (max.) |
| Weight | [Grams] | 35 |
| Physical Size (type.) | [mm] | 66.7(H) ×120.3(V) |
| Electrical Interface | | MIPI |
| Surface Treatment | | AG (3H) |
| Support Color | | 16.7M colors |
| Temperature Range<br>Operating<br>Storage (Non-Operating) | <br>[°C]<br>[°C] | <br>-20 to +70<br>-30 to +80 |
| RoHS Compliance | | RoHS Compliance |

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## 2.2 Display Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C (Room Temperature):

| Item | Unit | Conditions | Min. | Typ. | Max. | Note |
|---|---|---|---|---|---|---|
| White Luminance (LCD only) | [cd/m2] | $I_{LED}$= 25.4 mA (*2 parallels) (center point) | | 600 | | 1 |
| Uniformity | % | 5 points | 75 | | | 2,3 |
| Contrast Ratio | | | | 1000 | | 4 |
| Response Time | [msec] | Rising | | | | 5 |
| | [msec] | Falling | | | | |
| | [msec] | Rising + Falling | | 35 | | |
| Viewing Angle | [degree] [degree] | Horizontal (Right) CR = 10 (Left) | | 89 89 | | 6 |
| | [degree] [degree] | Vertical (Upper) CR = 10 (Lower) | | 89 89 | | |
| Color / Chromaticity Coordinates (CIE 1931) | | Red x | 0.591 | 0.641 | 0.691 | |
| | | Red y | 0.288 | 0.338 | 0.388 | |
| | | Green x | 0.250 | 0.300 | 0.350 | |
| | | Green y | 0.569 | 0.619 | 0.669 | |
| | | Blue x | 0.104 | 0.154 | 0.204 | |
| | | Blue y | 0.012 | 0.062 | 0.112 | |
| | | White x | 0.263 | 0.313 | 0.363 | |
| | | White y | 0.279 | 0.329 | 0.379 | |
| Color Gamut | % | | | 70 | | |

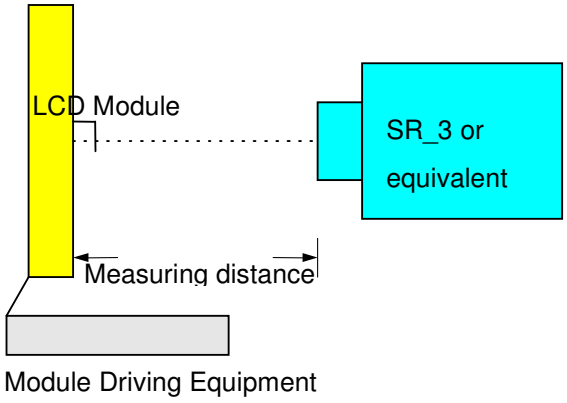
Note 1: Measurement method

1.1. Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

Aperture 1□with 50cm viewing distance

Test Point Center

Environment *< 1 lux*

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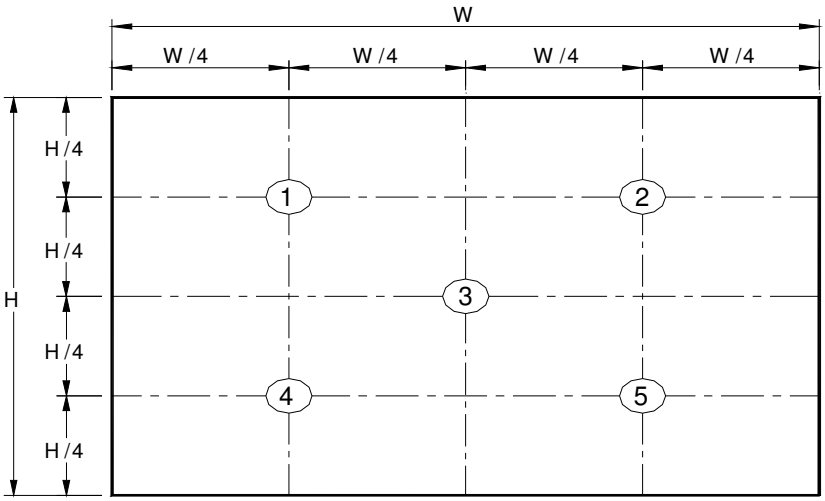
Note 2: Definition of 5 points position (Display active area: 62.1 x 110.4)




Note 3: The luminance uniformity of 5 points is defined by dividing the minimum luminance values by the maximum test point luminance

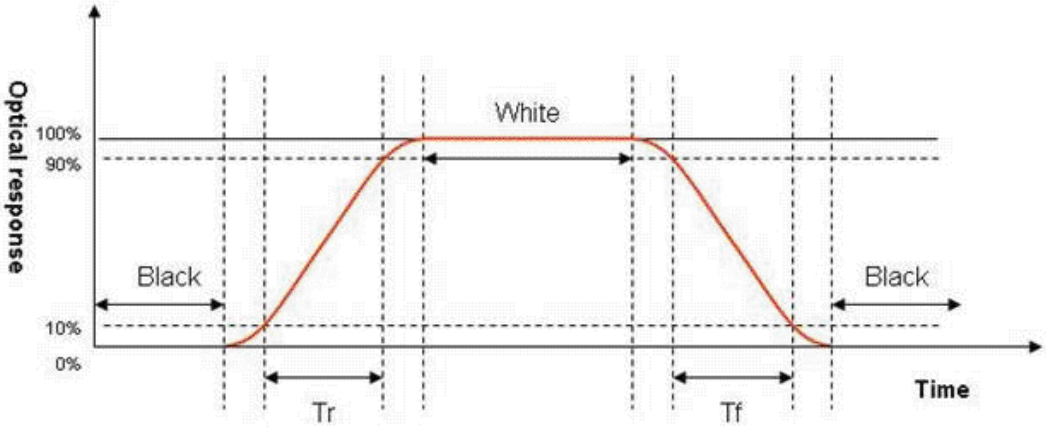
$$\delta_{W5} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

Note 5: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.

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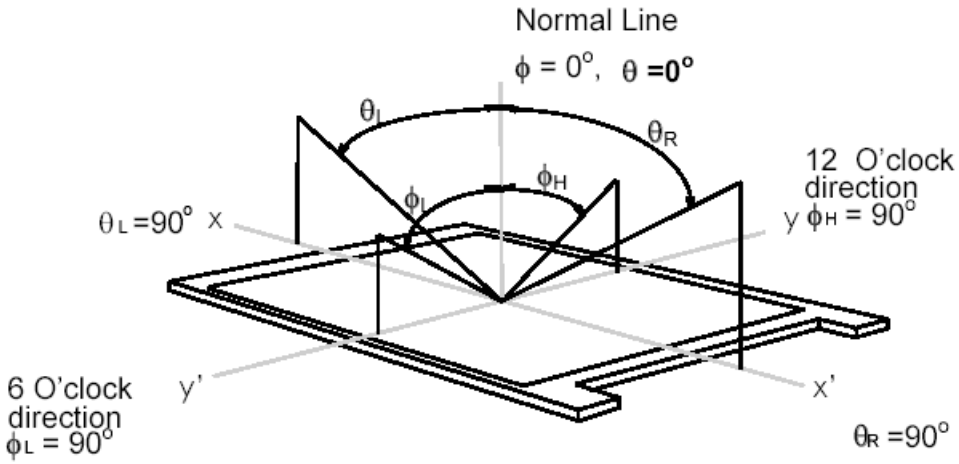
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.

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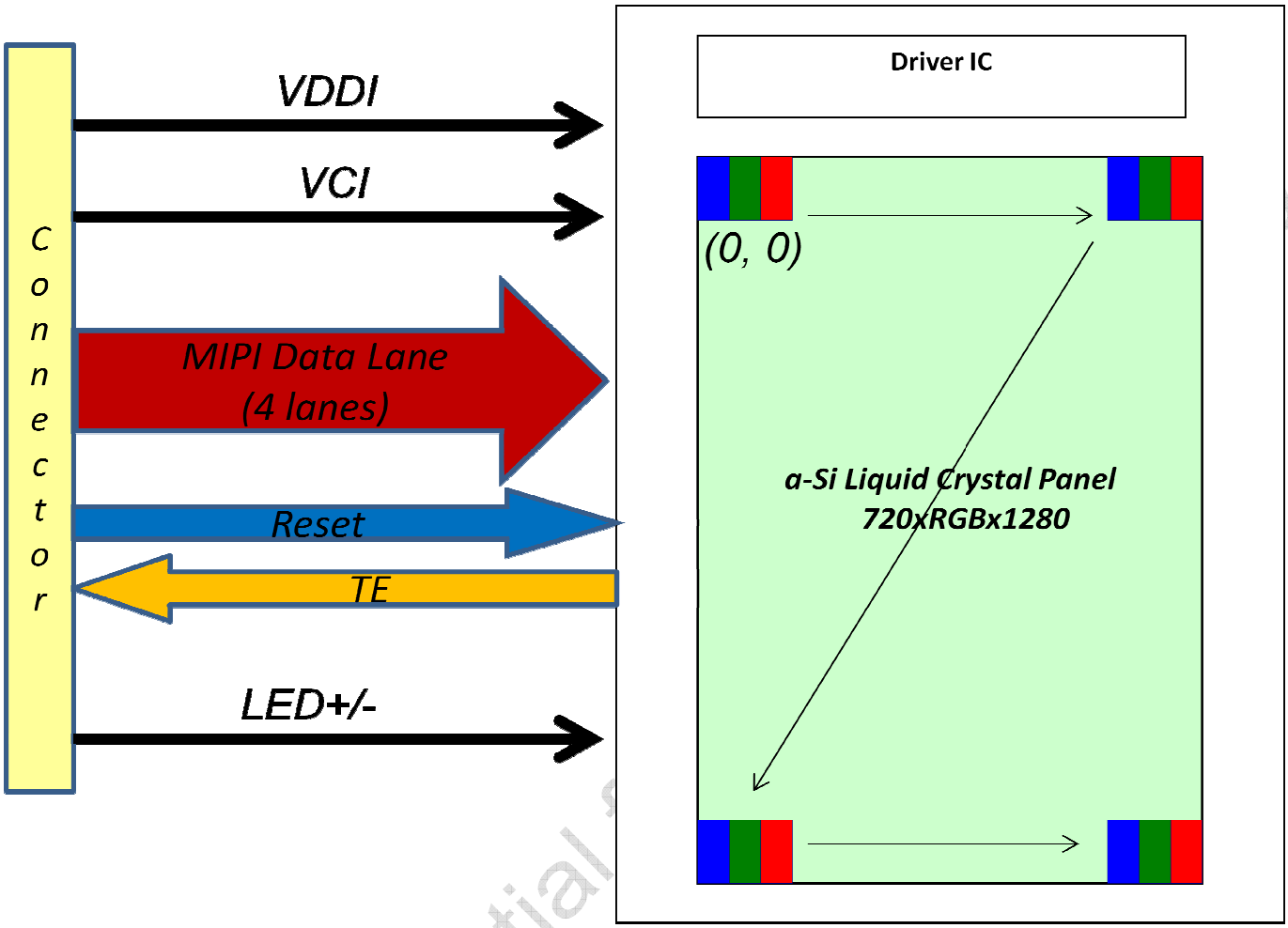
## 3. Functional Block Diagram

The following diagram shows the functional block of the 5 inch color TFT/LCD module:

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# 4. Absolute Maximum Ratings

## 4.1 Absolute Ratings of TFT LCD Module

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Logic Supply Voltage | VDDI | -0.3 | 5.5 | [Volt] |
| Analog Supply Voltage | VCI | -0.3 | 5.5 | [Volt] |

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

## 4.2 Absolute Ratings of Environment

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | TOP | -20 | 70 | [°C] |
| Storage Temperature | TST | -30 | 80 | [°C] |

Note: Maximum Wet-Bulb should be 39 °C and no condensation.

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# 5. Electrical Characteristics

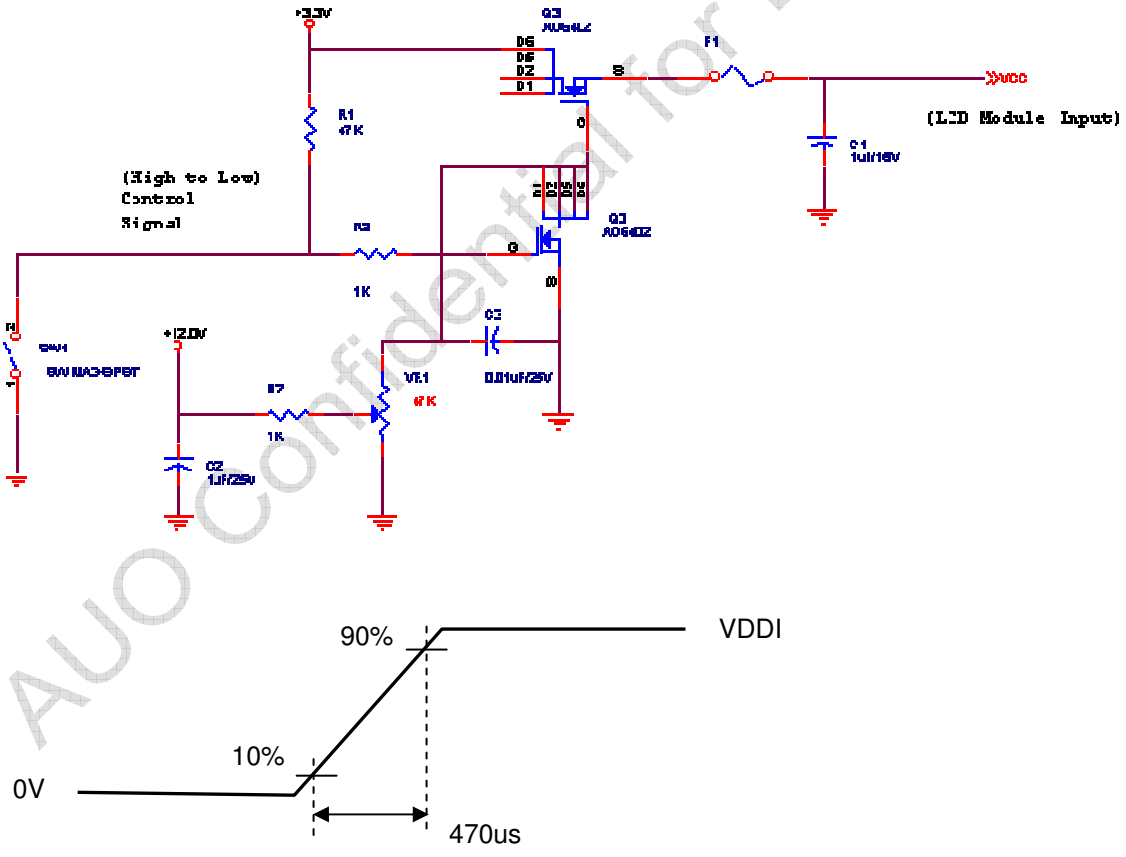
## 5.1 TFT LCD Module

### 5.1.1 Power Specification

Input power specifications are shown as follows;

| Symbol | Parameter | Min | Typ | Max | Units | Remark |
|---|---|---|---|---|---|---|
| VDDI | Logic Operating Voltage | 1.65 | 1.8 | 3.6 | [Volt] | |
| VCI | Analog Operating Voltage | 2.5 | 2.8 | 3.6 | [Volt] | Black Pattern (VDDI=1.8V, at 60Hz) |
| $I_{VDDI}$ | VDDI Current | - | 30 | 40 | [mA] | Note 1 |
| $I_{VCI}$ | VCI Current | - | 5 | 12 | [mA] | Note 1 |
| IRush | Inrush Current | | | 1500 | [mA] | |
| $P_{VCC}$ | VCC Power | - | 68 | 105.6 | [mWatt] | Black Pattern (VDDI=1.8V, VCI=2.8V, at 60Hz) |
| VDDIrp | Allowable Logic/LCD Drive Ripple Voltage | | | 100 | [mV] p-p | |

Note 1: Measurement condition:







**VDDI rising time**

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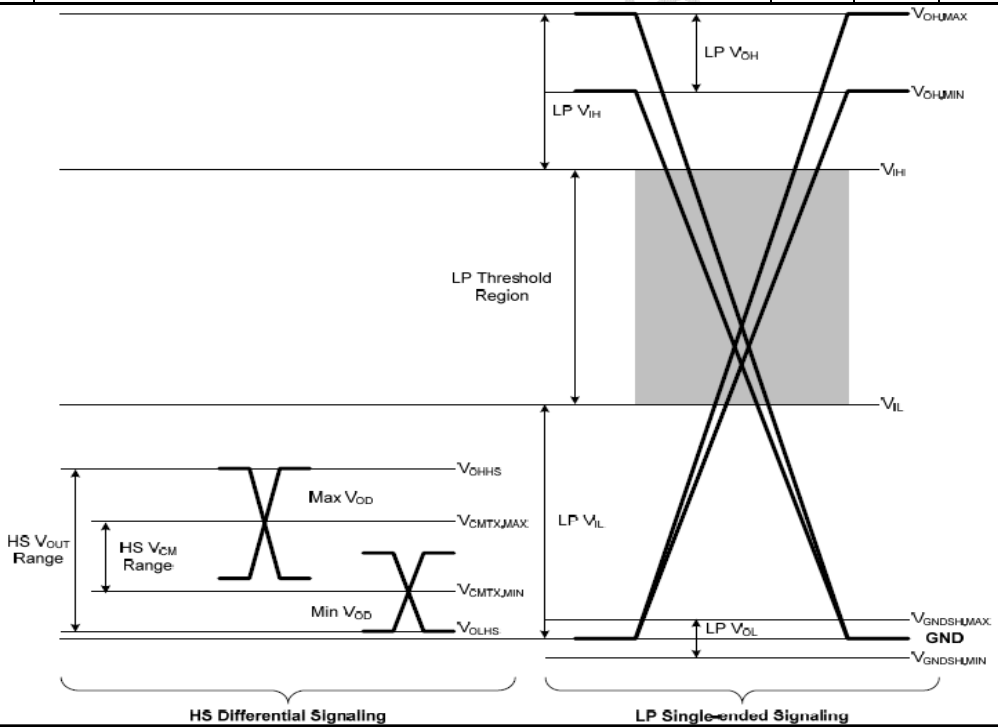
### 5.1.2 Signal Electrical Characteristics

- MIPI DC characteristics are as follows :

| MIPI Receiver Differential Input (DC Characteristics) | | | | | |
|---|---|---|---|---|---|
| Symbol | Parameter | Min | Typ | Max | Unit |
| $BR_{MIPI}$ | Input data bit rate | 200 | - | 1000 | Mbps |
| $V_{CMRX}$ | Common-mode voltage(HS Rx mode) | 155 | - | 330 | mV |
| $V_{IDTH}$ | Differential input high threshold (HS Rx mode) | - | - | 70 | mV |
| $V_{IDTL}$ | Differential input low threshold (HS Rx mode) | -70 | - | - | mV |
| $\lvert V_{IDM} \rvert$ | Differential input voltage range (HS Rx mode) | 70 | - | 500 | mV |
| $V_{IHHS}$ | Single-end input high voltage (HS Rx mode) | - | - | 460 | mV |
| $V_{ILHS}$ | Single-end input low voltage (HS Rx mode) | -40 | - | - | mV |
| $Z_{ID}$ | Differential input impedance | 80 | 100 | 125 | Ω |
| $V_{IHLP}$ | Logic 1 input voltage (LP Rx mode) | 880 | | | mV |
| $V_{ILLP}$ | Logic 0 input voltage (LP Rx mode) | | | 550 | mV |




| MIPI Receiver Differential Input (AC Characteristics) | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $\Delta V_{CMRX(HF)}$ | Common-mode interference beyond 450MHz | | - | - | 100 | mV |
| $\Delta V_{CMRX(LF)}$ | Common-mode interference 50MHz ~ 450MHz | | -50 | - | 50 | mV |
| $C_{CM}$ | Common-mode termination | | - | - | 60 | pF |
| $UI_{INST}$ | UI instantaneous | | 1 | | 12.5 | ns |

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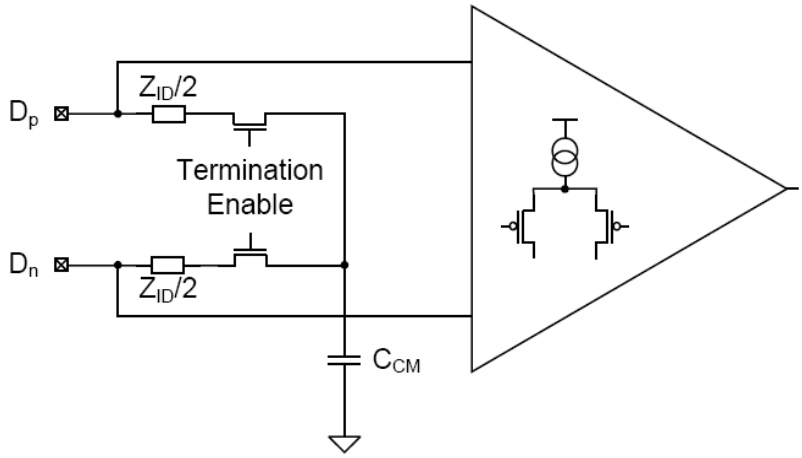
- HS RX Scheme

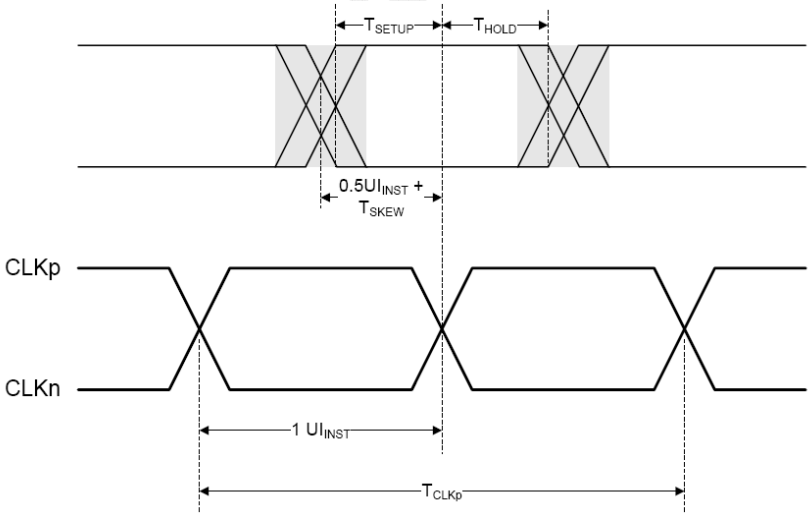



| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{SKEW[TX]}$ | Data to Clock Skew (mesured at transmitter) | -0.15 | | 0.15 | $UI_{INST}$ | 1 |
| $T_{SETUP[RX]}$ | Data to Clock Setup Time (receiver) | 0.25 | | | $UI_{INST}$ | 2 |
| $T_{HOLD[RX]}$ | Data to Clock Hold Time (receiver) | 0.25 | | | $UI_{INST}$ | 2 |

**Note:**

1. Total silicon and package delay budget of 0.25*$UI_{INST}$
2. Total setup and hold window for receiver of 0.5 *$UI_{INST}$

- High Speed Data Transmission: Data to Clock Timing




| LP Receiver AC Specifications | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $e_{SPIKE}$ | Input pulse rejection | | - | - | 300 | V · ps |
| $T_{MIN-RX}$ | Minimum pulse width response | | 50 | - | - | ns |
| $V_{INT}$ | Peak interference amplitude | | - | - | 200 | mV |
| $f_{INT}$ | Interference frequency | | 450 | - | - | MHz |

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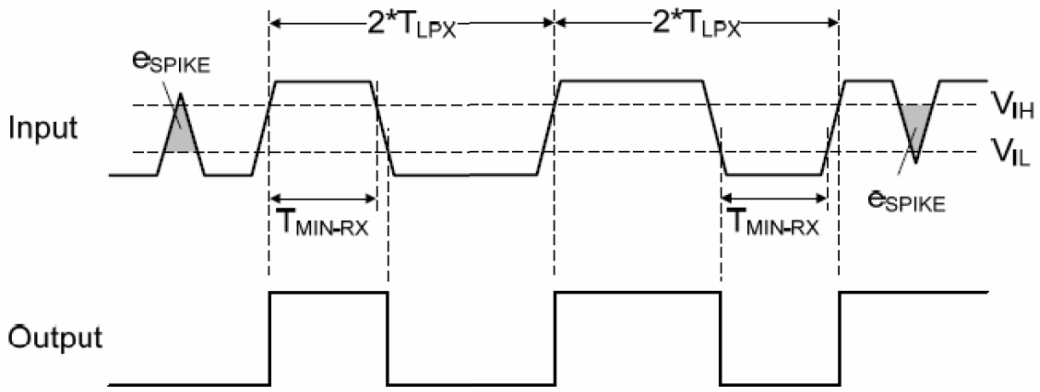
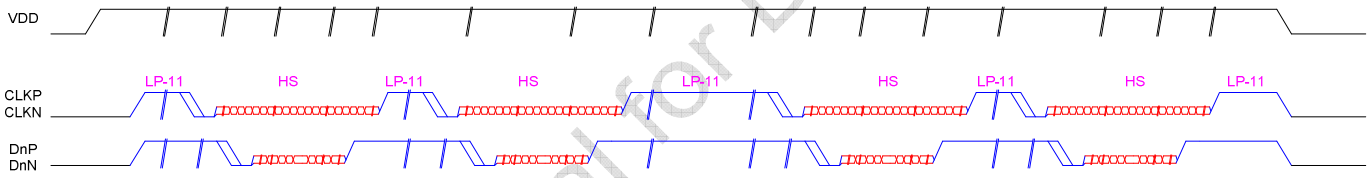
- Input Glitch Rejection of Low-Power Receivers




For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.




The timing definitions are listed in below,

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TCLK-MISS | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX. | | | 60 | ns |
| TCLK-POST | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL. | 60 ns + 52*UI | | | ns |
| TCLK-PRE | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI |
| TCLK-PREPARE | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns |
| TCLK-SETTLE | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from | 95 | | 300 | ns |

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| | | | | | |
|---|---|---|---|---|---|
| | the beginning of TCLK-PREPARE. | | | | |
| TCLK-TERM-EN | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX. | | | 38 | ns |
| TCLK-TRAIL | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns |
| TCLK-PREPARE + TCLK-ZERO | TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns |
| TD-TERM-EN | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX. | | | 35 ns + 4*UI | ns |
| TEOT | Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst. | | | 105 ns + 12*UI | ns |
| THS-EXIT | Time that the transmitter drives LP-11 following a HS burst. | 100 | | | ns |
| THS-SYNC | HS Sync-Sequence '00011101' period | | 8 | | UI |
| THS-PREPARE | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40 ns + 4*UI | | 85 ns + 6*UI | ns |
| THS-PREPARE + THS-ZERO | THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145 ns + 10*UI | | | ns |
| THS-SETTLE | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. | 85 ns + 6*UI | | 145 ns + 10*UI | ns |
| THS-SKIP | Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst. | 40 | | 55 ns + 4*UI | ns |
| THS-TRAIL | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | 60 ns + 4*UI | | | ns |
| TLPX | Transmitted length of any Low-Power state period | 50 | | | ns |
| Ratio TLPX | Ratio of TLPX(MASTER)/TLPX(SLAVE) | 2/3 | | 3/2 | |

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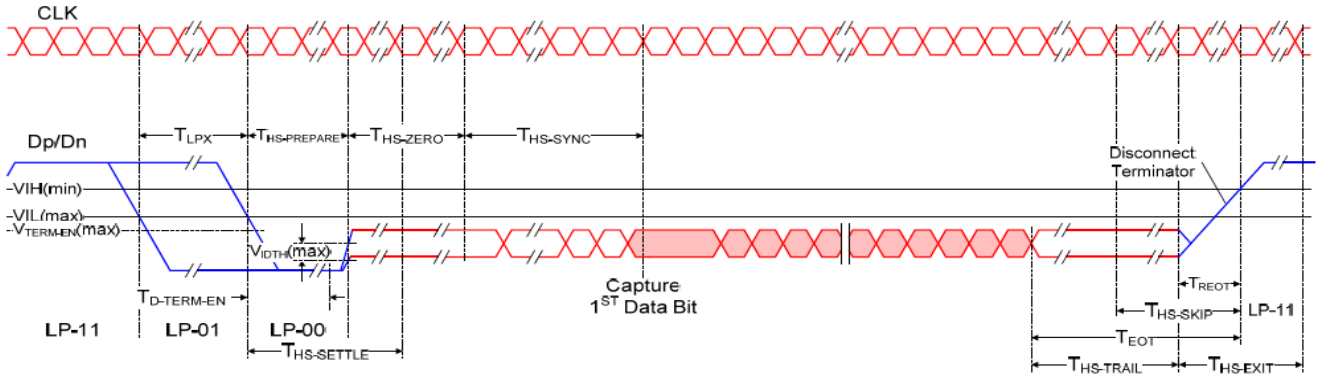
| | | | | | |
|---|---|---|---|---|---|
| | between Master and Slave side | | | | |
| TTA-GET | Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | | 5*TLPX | | ns |
| TTA-GO | Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | | 4*TLPX | | ns |
| TTA-SURE | Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | TLPX | | 2*TLPX | ns |

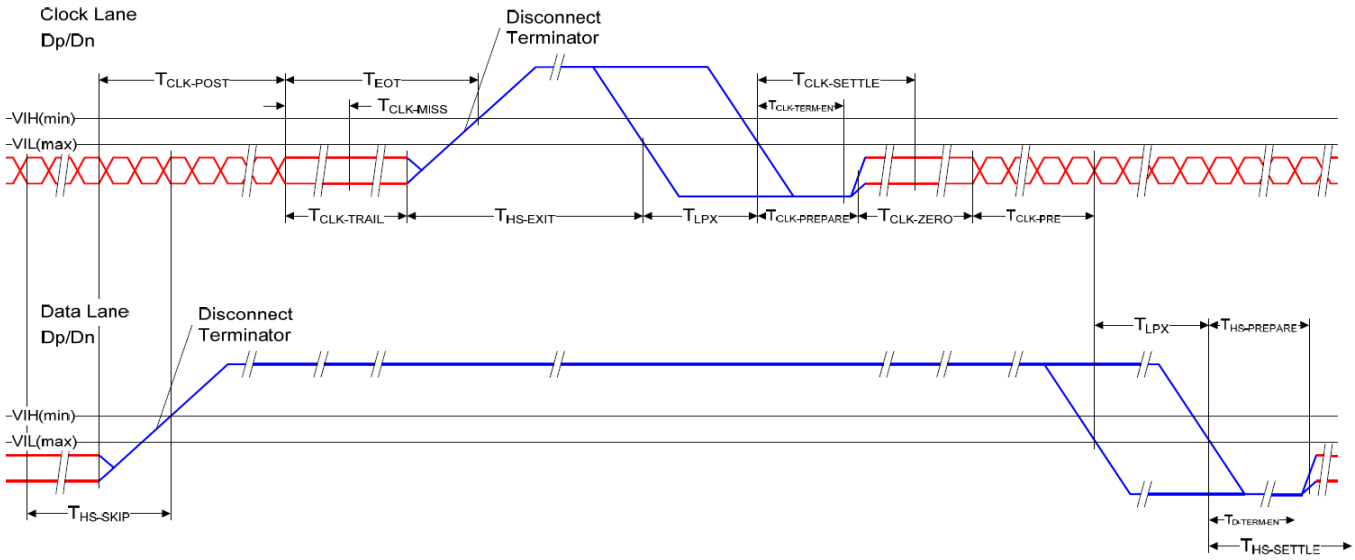
**Note:**

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
3. The I-chip of AUO use is not support BTA (BTA define ignore).

- High-Speed Data Transmission in Bursts




- Switching the Clock Lane between Clock Transmission and Low-Power Mode

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## 5.2 Backlight Unit

### 5.2.1 Parameter guideline for LED

Following characteristics are measured under a stable condition using an inverter at 25□ (Room Temperature):

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| **IF** | LED Forward Current | - | 25.4 | - | mA | Ta = 25°C<br>50.8mA for 2 parallel |
| **VLED** | LED Forward Voltage | - | 14.25 | 15.5 | [Volt] | $I_F$ = 25.4mA, Ta = 25°C |
| **PLED** | LED Power Consumption | - | 0.73 | - | Watt | $I_F$ = 25.4mA, Ta = 25°C<br>w/o efficiency |
| **LED life time** | | 10,000 | - | - | Hrs | $I_F$ = 25.4 mA, Ta = 25°C |

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: IF, VLED , PLED are defined for LED Light Bar. There is two LED channel (AN1-CA1, AN2-CA2) in back light unit.

Note 3: If G050TAN01.0 module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 4: Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

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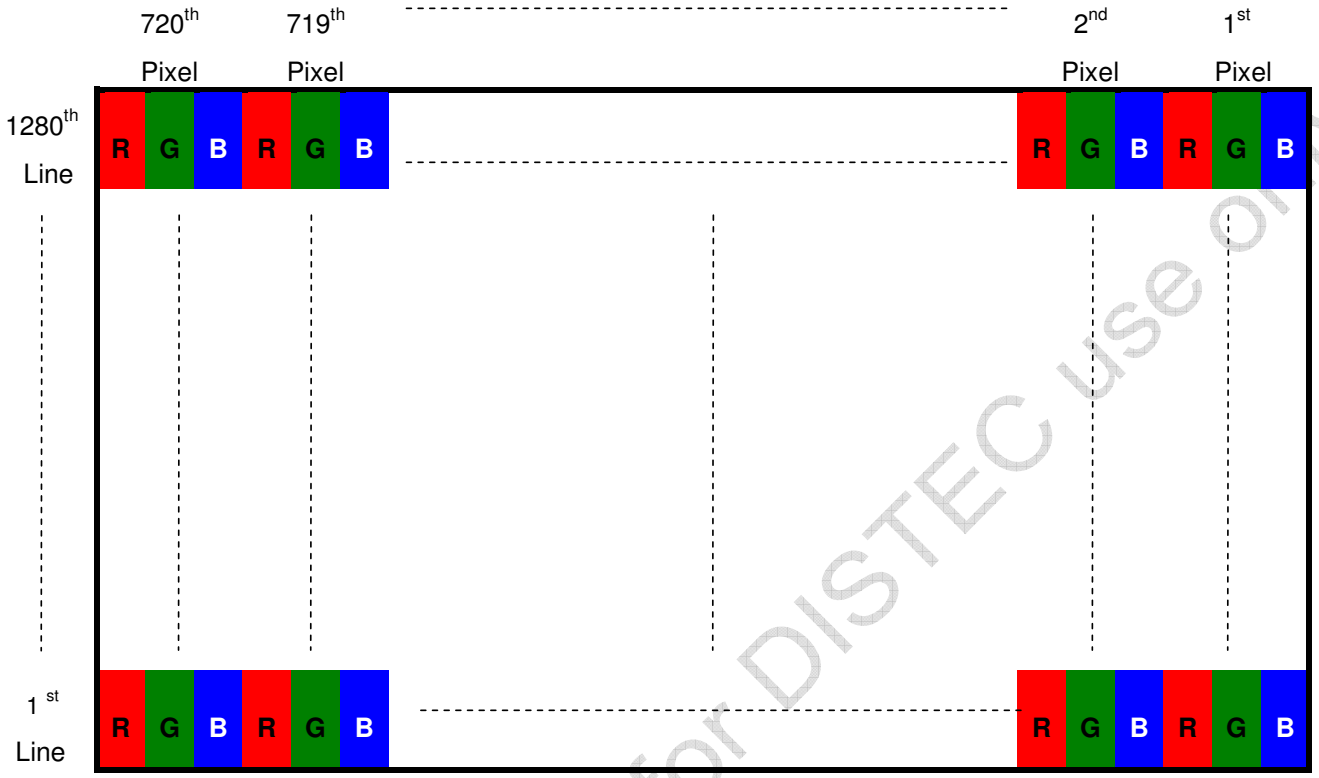
# 6. Signal Characteristic

## 6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.

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## 6.2 Signal Description

### 6.2.1 LCD MIPI Interface pin description

| Connector Name / Designation | Signal Connector |
|---|---|
| Manufacturer | MOLEX or compatible |
| Connector Model Number | 55650-0388 or compatible |
| Mating Model Number | 54363-0389 or compatible |

| Pin no | Symbol | Description | Remark |
|---|---|---|---|
| 1 | D0- | DSI_D0- differential data signal | |
| 2 | GND | Ground | |
| 3 | D0+ | DSI_D0+ differential data signal | |
| 4 | NC | | |
| 5 | GND | Ground | |
| 6 | TE | Frame head pulse signal | |
| 7 | D1- | DSI_D1- differential data signal | |
| 8 | RESET | | |
| 9 | D1+ | DSI_D1+ differential data signal | |
| 10 | NC | | |
| 11 | GND | Ground | |
| 12 | VDDI | I/O supply voltage range 1.65V~3.6V | |
| 13 | CLK- | DSI_CLK- differential data signal | |
| 14 | GND | Ground | |
| 15 | CLK+ | DSI_CLK+ differential data signal | |
| 16 | VCI | Analog supply voltage range 2.5V~3.6V | |
| 17 | GND | Ground | |
| 18 | GND | Ground | |
| 19 | D2- | DSI_D2- differential data signal | |
| 20 | LED_A1 | LED+ | |
| 21 | D2+ | DSI_D2+ differential data signal | |
| 22 | LED_A2 | LED+ | |
| 23 | GND | Ground | |
| 24 | LED_C1 | LED- | |
| 25 | D3- | DSI_D3- differential data signal | |
| 26 | LED_C2 | LED- | |
| 27 | D3+ | DSI_D3+ differential data signal | |
| 28 | GND | Ground | |
| 29 | GND | Ground | |
| 30 | GND | Ground | |

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## 6.3 Interface Timing

- **Timing Characteristics**

Basically, interface timings should match the 720 x 1280 /60 Hz manufacturing guide line timing.

| ITEM | | | SYNBOL | min | typ | max | UNIT |
|---|---|---|---|---|---|---|---|
| LCD | Frame Rate | | - | | 60 | | Hz |
| Timing | DCLK | Frequency | fCLK | | 77.94 | | MHz |
| | | Period | Tclk | 1 | | | ns |
| | Horizontal | Horizontal total time | tHP | | 976 | | $t_{CLK}$ |
| | | Horizontal Active time | tHadr | | 720 | | $t_{CLK}$ |
| | | Horizontal Pulse Width | tHsync | | 128 | | $t_{CLK}$ |
| | | Horizontal Back Porch | tHBP | | 72 | | $t_{CLK}$ |
| | | Horizontal Front Porch | tHFP | | 56 | | $t_{CLK}$ |
| | Vertical | Vertical total time | tvp | | 1331 | | $t_H$ |
| | | Vertical Active time | tVadr | | 1280 | | $t_H$ |
| | | Vertical Pulse Width | tVsync | | 10 | | $t_H$ |
| | | Vertical Back Porch | tVBP | | 38 | | $t_H$ |
| | | Vertical Front Porch | tVFP | | 3 | | $t_H$ |
| Differential Swing | | | VDswing | 140 | | | mV |
| Bit Rate | | | TX SPD (MBPS) | | 500 | | Mbps |
| Pixel Fomat | | | | | 8 | | Data bit/ pixel |
| Lane | | | | | 4 | | Lane |

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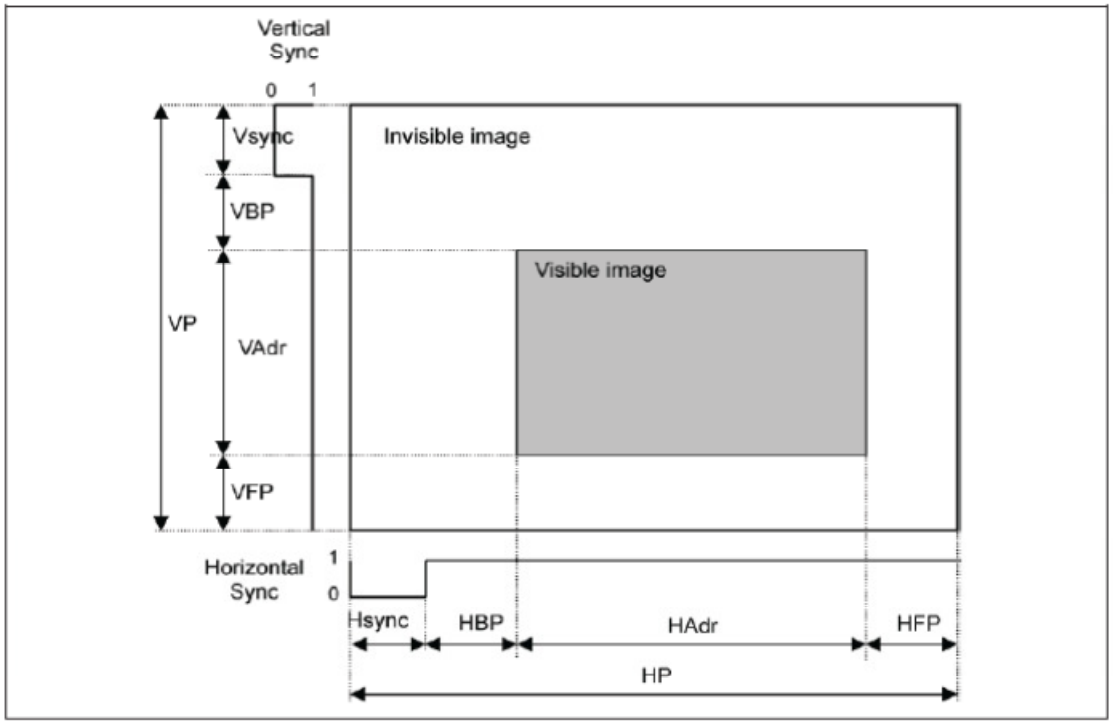


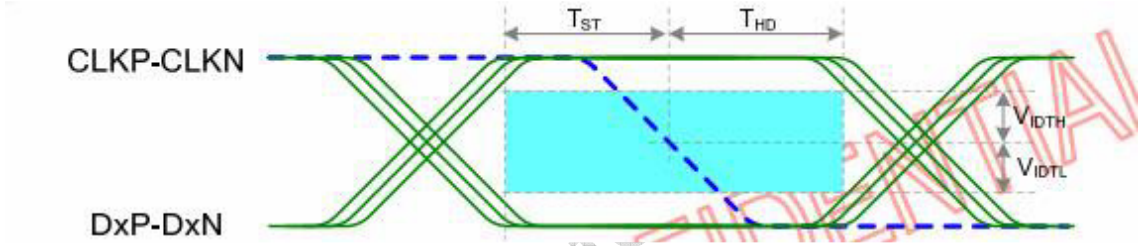


**Note:** VIDTH is the input high threshold and should >70mV

VIDTL is the input low threshold and should < -70mV

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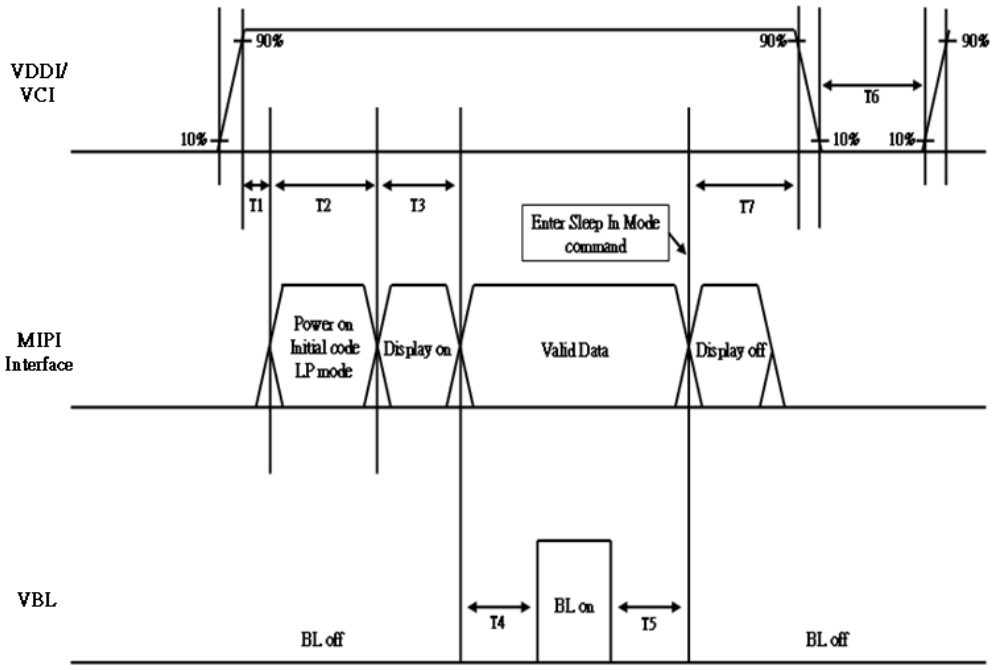
## 6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.




| Parameter | Value | | | | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Unit | |
| T1 | 20 | - | - | ms | |
| T2 | 120 | - | - | ms | |
| T3 | 10 | - | - | ms | |
| T4 | 200 | - | - | ms | |
| T5 | 110 | - | - | ms | |
| T6 | 500 | - | - | ms | |
| T7 | 60 | - | - | ms | |

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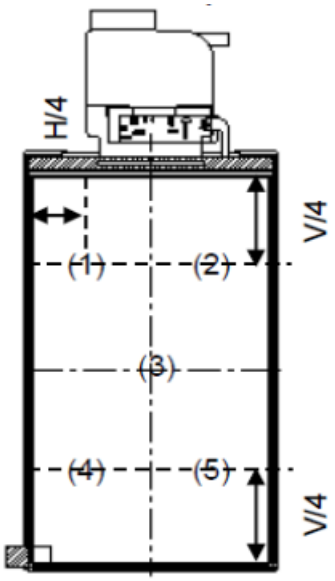
# 7. Reliability Test Criteria

| Items | Required Condition | Note |
|---|---|---|
| Temperature Humidity Bias | 60 °C, 90%RH, 240 hours | |
| High Temperature Operation | 70 °C, 240 hours | |
| Low Temperature Operation | -20 °C, 240 hours | |
| Hot Storage | 80 °C, 240 hours | |
| Cold Storage | -30 °C, 240 hours | |
| Thermal Shock Test | -20 °C / 30 min, 70 °C / 30 min, 100cycles, 40 °C minimun ramp rate | |
| Shock Test (Non-Operating) | 50G, 20ms, Half-sine wave, ( ±X, ±Y, ±Z) | |
| Vibration Test (Non-Operating) | 1.5G, (10~200Hz, Sine wave)<br>30 mins/axis, 3 direction (X, Y, Z) | |
| ESD | TBD | |
| EMI | TBD | |

Note1: ESD Criteria.




Note2:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.
- In the standard condition, there is not display function NG issue occurred.

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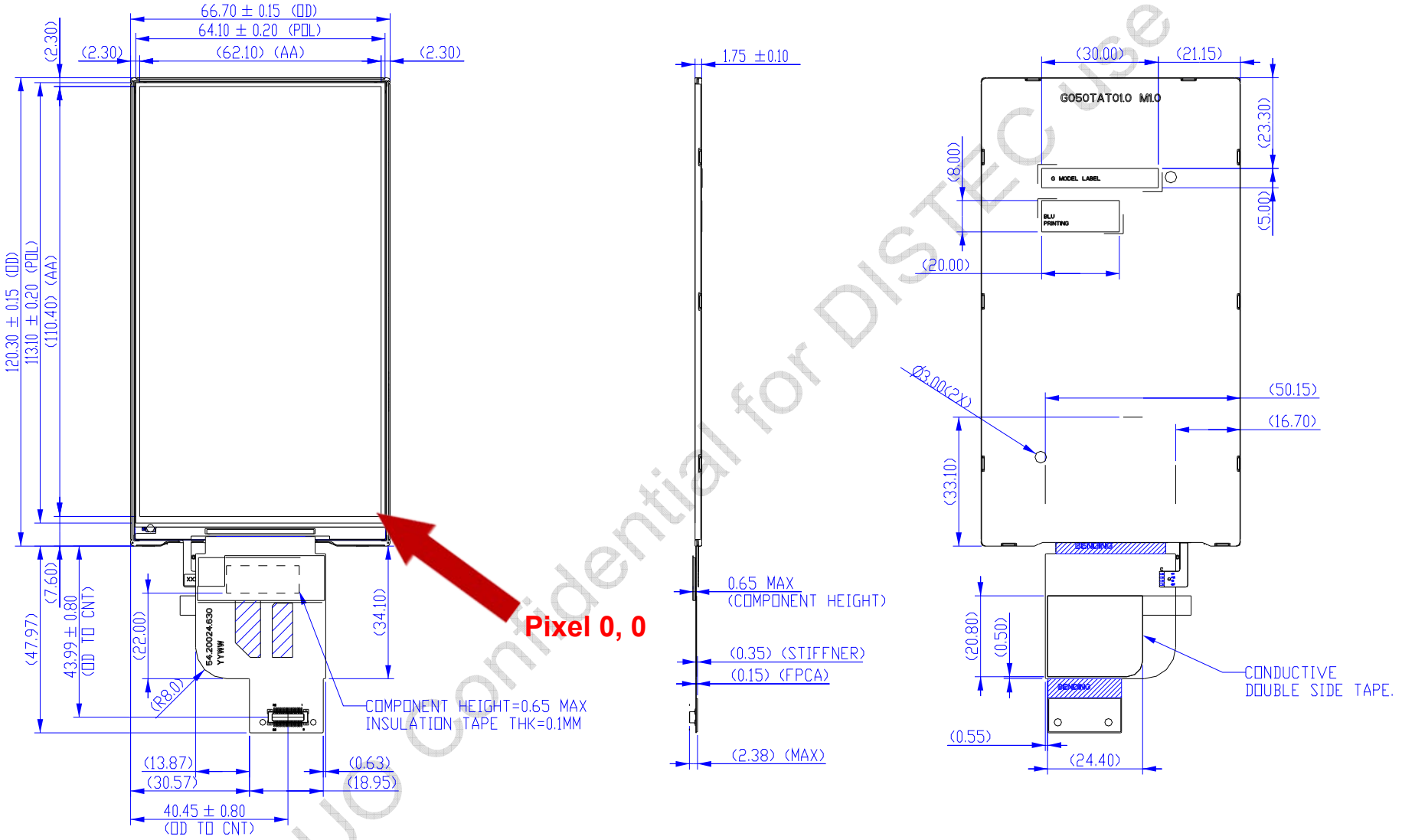
# 8. Mechanical Characteristics

## 8.1 Total Solution Outline Dimension

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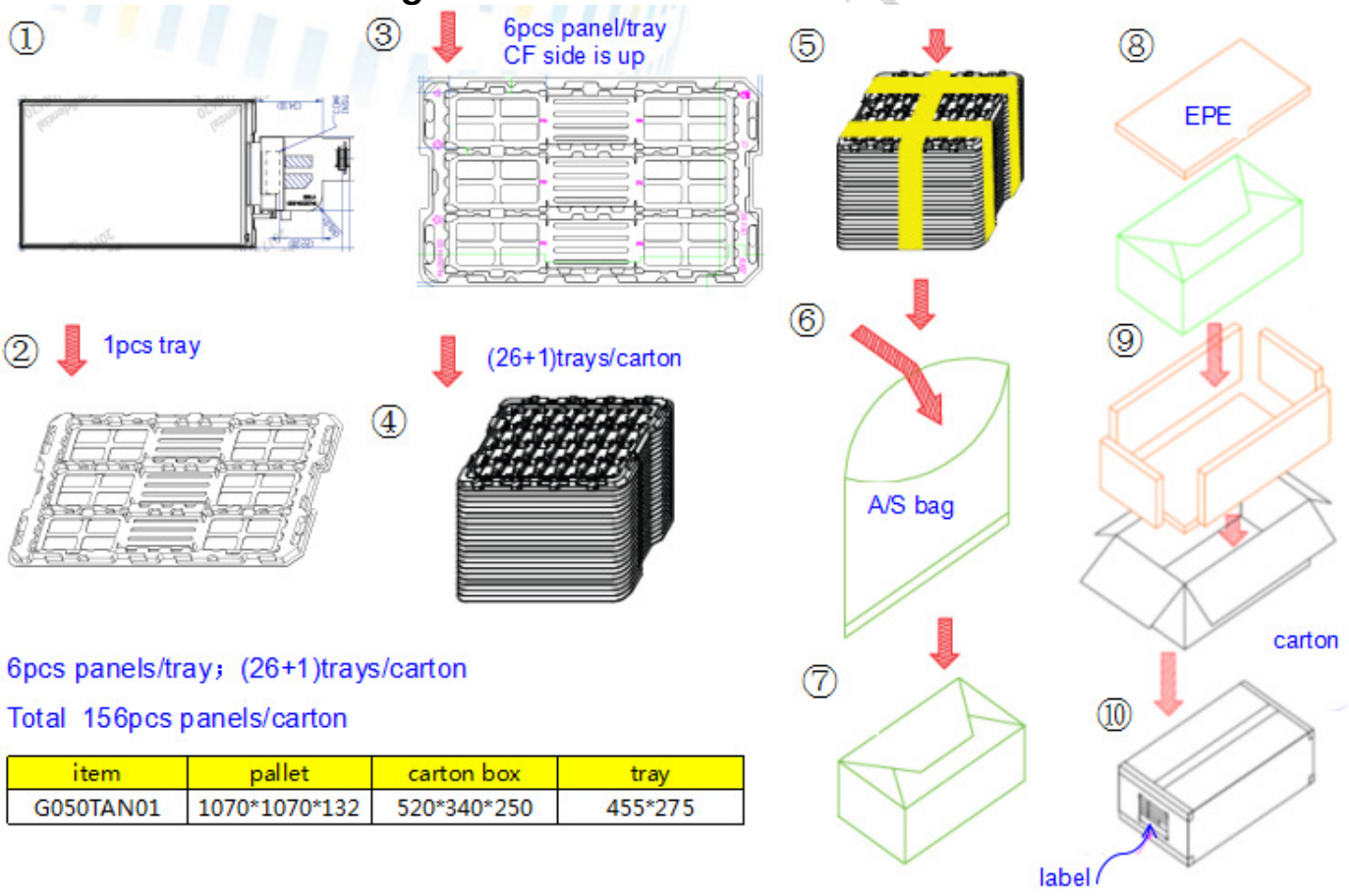
# 9. Label and Packaging

## 9.1 Shipping Label (on the rear side of TFT-LCD display)

Label 大小：30mm*5mm


## 9.2 Carton/Pallet Package




6pcs panels/tray；(26+1)trays/carton

Total 156pcs panels/carton

| item | pallet | carton box | tray |
|---|---|---|---|
| G050TAN01 | 1070*1070*132 | 520*340*250 | 455*275 |

# 10 Safety

## 10.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

## 10.2 Materials

### 10.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

### 10.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process.

The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

## 10.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

## 10.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

| | |
|---|---|
| UL 60950-1 second edition | U.S.A. Information Technology Equipment |

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