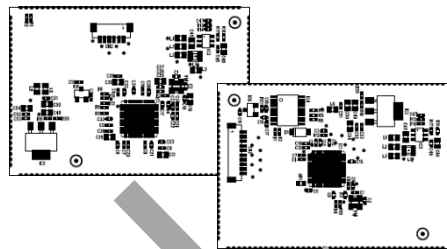


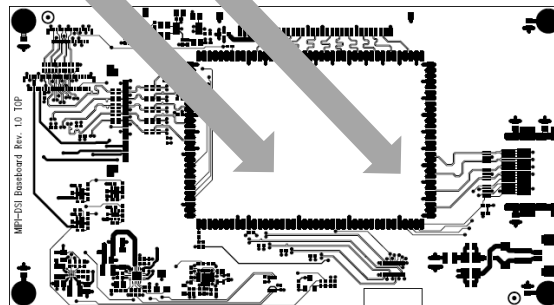
Datasheet

PrismaMIPI-HDMI PrismaMIPI-LVDS

Functional



MEET



Display

Version 1.0

April 24th, 2018

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Revision History

Date	Rev	Description	Page
April, 2018	1.0	First draft	

1 General Description

The Prisma MIPI-DSI-Bridging provides a cost-effective solution for connecting LCD-TFT displays with MIPI-DSI interface to conventional digital video interfaces. To ensure maximum flexibility, the PrismaMIPI is designed as a BridgeModule – BaseBoard combination. The basic conversion functionality is mapped on the BridgeModule and the display specific mechanical and electrical adjustments are implemented on the baseboard.

2 Concept - Setup

2.1 BridgeModule - BM

The BM has various digital video interfaces with a fixed arrangement. Which video interface acts as input and which as output is only defined by the bridge component itself. It is designed in plated half-hole technology which allows simple and cheap board-to-board connection without any additional connectors.

The following picture shows a sample for half-hole technology

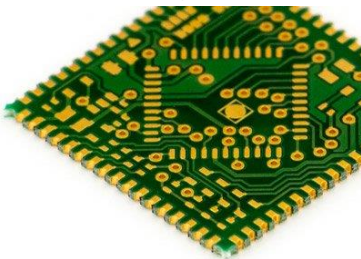


Fig. 1

Fig.2 shows the available video interfaces and their arrangement on the BM.

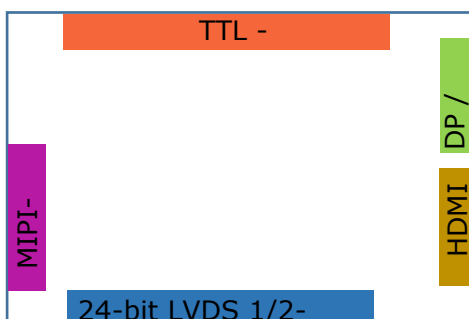


Fig. 2

Besides the video interfaces also further interfaces (audio, UART, I2C) and signals are defined.

For further details please see Appendix-BM.

Available BridgeModules

Currently the following BridgeModules are available.

- HDMI-to-MIPI-DSI
- LVDS-to-MIPI-DSI

Besides the currently available BridgeModules further BMs are possible. Please see the following diagram. For availability please contact your local sales person.

		Display Interface (Output)			
		TTL	LVDS	eDP	MIPI-DSI
Host / Board (Input)	TTL		1)	✓	✓
	LVDS	1)		✓	✓
	HDMI 1.4	✓	✓	✓	✓
	eDP/DP	✓	✓		✓
	MIPI-DSI		✓	✓	

1)Not reasonable for BM

2.2 BaseBoard - BB

Available MIPI-DSI displays do not follow any standard regarding

- connector-type
- connector location
- required logic power-supply/-ies
- required power-on sequencing
- backlight
- etc.

For this reason all display specific details are realized on the BB, which is a simple, cheap 2- or 4-layer PCB-board. Besides the display specific features also the input interface can be adapted to any requirements very easily.

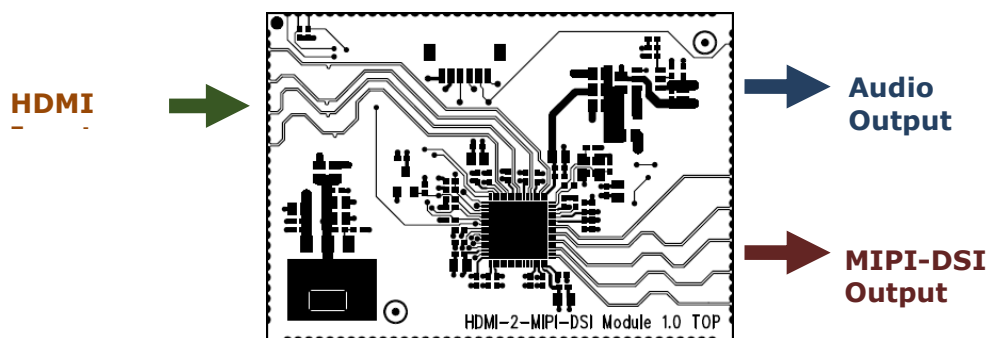
The currently available **BB-I** supports the following displays

- Ortustech COM48H4N22ULC
- Ortustech COM50H5N03ULC
- Ampire AM-7201280HTZQW-00H
- AUO G080UAN01.0(00)

3. Bridge-Modules

3.1 HDMI-to-MIPI-DSI

The HDMI-to-MIPI-DSI BM is based on a high performance HDMI1.4 to MIPI®DSI bridge chip. The bridge deserializes input HDMI signal, decodes packets and converts the formatted video data stream to MIPI-DSI transmitter output. It features configurable single-port MIPI®DSI with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 1.5Gb/s/lane, which can support a total bandwidth of up to 6Gbps.



3.1.1 Features

HDMI 1.4 Receiver

- Compliant to the HDMI 1.4 specification with TMDS data rates up to 3.4Gbps per channel
- Support HDCP 1.4
- Adaptive receiver Equalization for PCB, cable and connector losses

MIPI-DSI Transmitter

- Compliant with DCS1.02, D-PHY1.2& DSI1.02 & CSI-2 1.0
- 1 Clock Lane, and 1~4 Configurable Data Lanes per port
- 80Mb/s~1.5Gb/s per Data Lane
- Burst Mode and Command Mode supported
- Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 20-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2, 12-bit YCbCr4:2:0 Video Format

Miscellaneous

- Internal CSC support conversions between YCbCr 4:4:4 and RGB, and between YCbCr 4:2:2 and YCbCr 4:4:4
- Support SPDIF and 8-channel IIS audio output (optional)

3.1.2 Electrical and environmental characteristics

Operating Values

Item	Condition	MIN.	TYP.	MAX.	Unit	Note
Supply Voltage ¹⁾		4.5	5.0	5.5	VDC	Single Supply
Current Input	Stand-by		TBD		mA	MIPI-DSI Output Resolution
	720x1280		TBD		mA	
	1200x1920		TBD		mA	
					mA	
					mA	

Temperature & Humidity

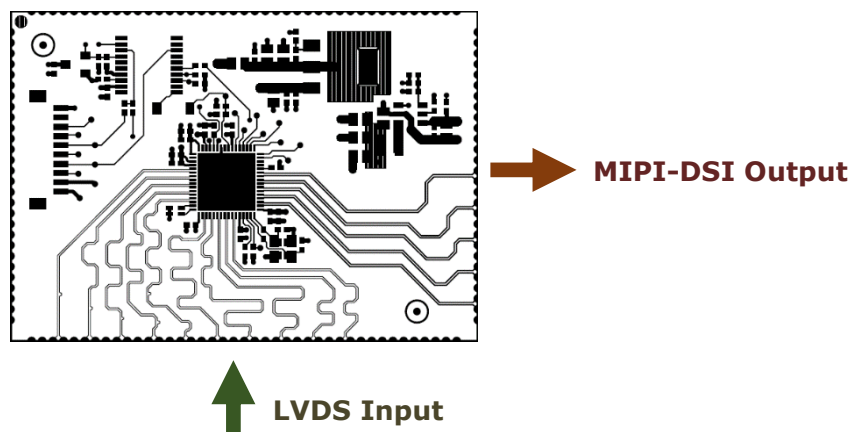
Item	MIN.	TYP.	MAX.	Unit	Note
Operating Temperature	-40	+27	85	°C	Free Air
Storage Temperature	-40	-	+125	°C	
Humidity		-	95	%RHmax	

3.1.3 Pin Assignment

Please see [Appendix: BM HDMI-to-MIPI-DSI](#)

3.2 LVDS-to-MIPI-DSI

The LVDS-to-MIPI-DSI BM is based on a high performance Single/Dual-Port LVDS to MIPI-DSI bridge chip. The bridge deserializes input LVDS signal, decodes packets and converts the formatted video data stream to MIPI-DSI transmitter output. It features a single port MIPI DSI transmitter with 1 high-speed clock lane and 1~4 configurable high-speed data lanes operating at maximum 1.5Gb/s/lane, which can support a total bandwidth of up to 6Gb/s.



3.2.1 Features

Single/Dual-Port LVDS Receiver

- Supports VESA and JEIDA standard
- 1~2 configurable port
- 1 clock lane and 3/4 data lanes per port
- Support Maximum Data Rate 1.2Gb/s/lane
- Resolution up to 1080P 60Hz for dual-port mode
- Input color depth supports 6-bit or 8-bit
- Support input De-SSC (30kHz +/- 5%)

Single-Port MIPI DSI Transmitter

- Compliant with DCS1.02, D-PHY1.1 & DSI1.02
- 1 Clock Lane and 1~4 Configurable Data Lanes
- 80Mb/s~1.5Gb/s per Data Lane
- Resolution Up to 1080P 60Hz
- Supports Non-Burst and Burst Video Mode
- Supports RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format

3.2.2 Electrical and environmental characteristics

Operating Values

Item	Condition	MIN.	TYP.	MAX.	Unit	Note
Supply Voltage ¹⁾		4.5	5.0	5.5	VDC	Single Supply
Current Input	Stand-by		TBD		mA	MIPI-DSI Output Resolution
	720x1280		TBD		mA	
	1200x1920		TBD		mA	
					mA	
					mA	

Temperature & Humidity

Item	MIN.	TYP.	MAX.	Unit	Note
Operating Temperature	-40	+27	85	°C	Free Air
Storage Temperature	-55	-	+125	°C	
Humidity		-	95	%RHmax	

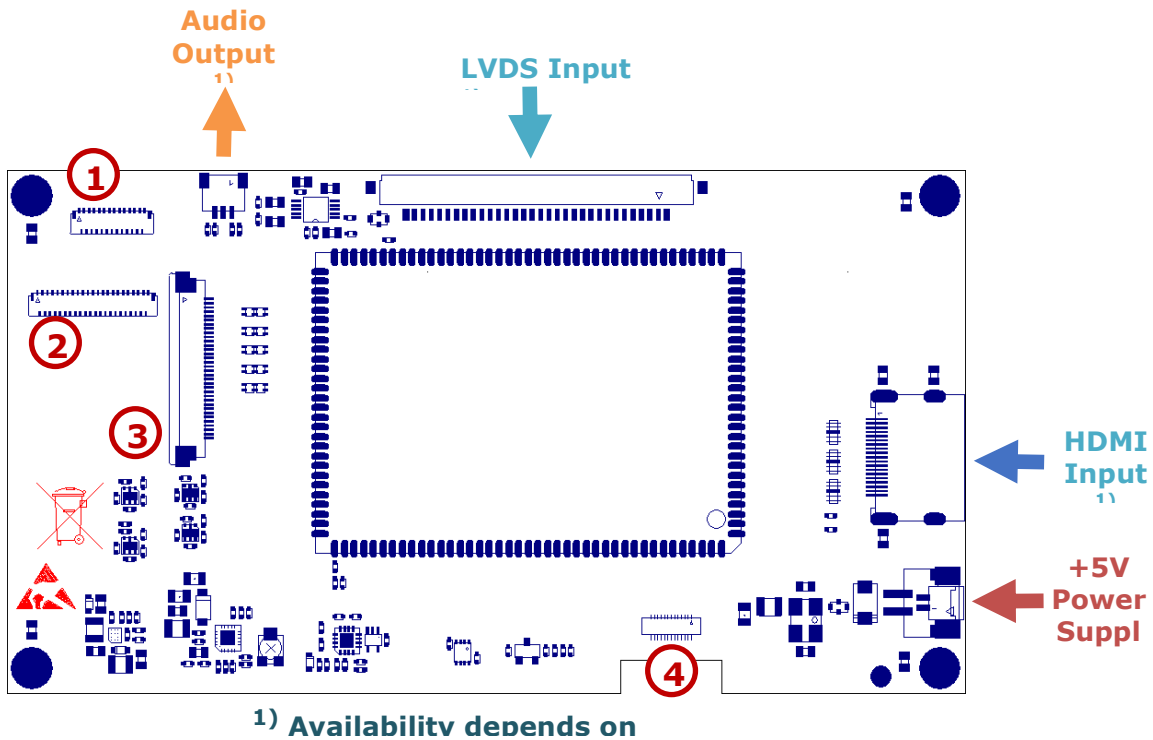
3.2.3 Pin Assignment

Please see Appendix: [BM LVDS-to-MIPI-DSI](#)

4 BaseBoard: B-I

4.1 Supported Displays and associated connector

The BaseBoard B-1 is designed so that it can be placed right behind each display. It must be taken into account that the corresponding assembly variant is required for each displays



①	Ortustech	COM50H5N03ULC	CN3
②	AUO	G080UAN01.0(00)	CN1
③	Ampire	AM-7201280HTZQW-00H	CN2
④	Ortustech	COM48H4N22ULC	CN11

4.2 Supported Feature per Display

Ortustech - COM48H4N22ULC

- VCC & IOVCC power supply
- Power-on sequencing and Reset control
- Backlight power supply
- Temperature-dependent LED current control

Ortustech - COM50H5N03ULC

- IOVCC, AVDD, AVEE power supply
- Power-on sequencing and Reset control
- Backlight power supply
- Temperature-dependent LED current control

Ampire - AM-7201280HTZQW-00H

- IOVCC, AVDD, AVEE power supply
- Power-on sequencing and Reset control
- Backlight power supply
- Temperature-dependent LED current control

AUO - G080UAN01.0(00)

- VCC power supply
- Backlight power supply

4.3 Electrical and environmental characteristics

Operating Values

Item	Condition	MIN.	TYP.	MAX.	Unit	Note
Supply Voltage		4.5	5.0	5.5	VDC	Single Supply
Current Input	Ortustech COM48H4N22ULC		TBD		mA	
	Ortustech COM50H5N03ULC		TBD		mA	
	Ampire AM-7201280HTZQW-00H		TBD		mA	
	AUO G080UAN01.0(00)		TBD		mA	

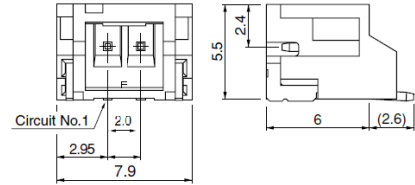
Temperature & Humidity

Item	MIN.	TYP.	MAX.	Unit	Note
Operating Temperature	-40	+25	+80	°C	Free Air
Operating Temperature with equipped audio option	-10	+25	+70	°C	
Storage Temperature	-55	-	+125	°C	
Humidity		-	95	%RHmax	

4.4 Connectors

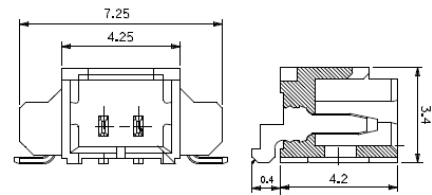
CN9 Power Supply Connector (optional)

Pin	Signal	Description
1	+5V	5V Power supply
2	GND	Ground



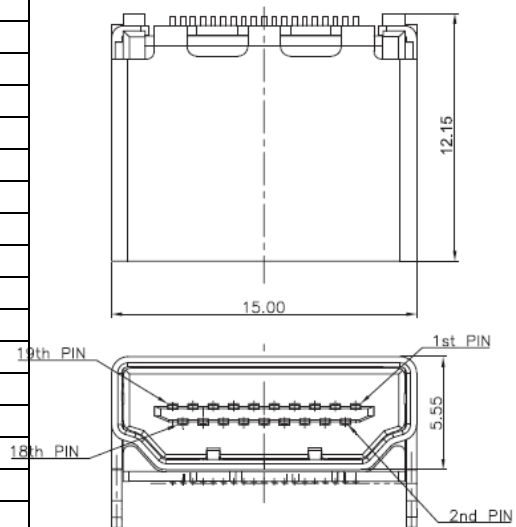
CN10 Power Supply Connector

Pin	Signal	Description
1	+5V	5V Power supply
2	GND	Ground



CN7 HDMI Input

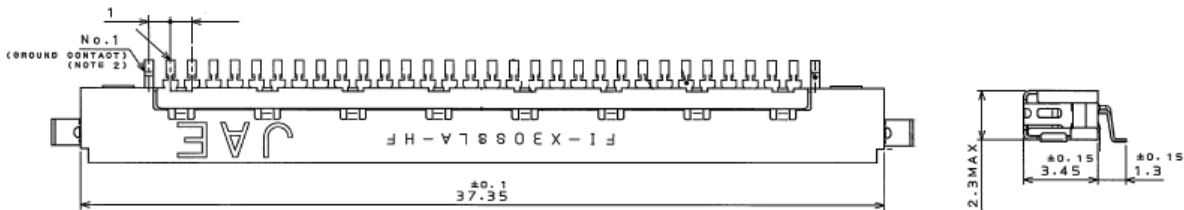
Pin	Signal	Description
1	TMDS2+	Differential TMDS Data 2+
2	TMDS2_SHLD	TMDS Data2 Shield
3	TMDS2-	Differential TMDS Data 2-
4	TMDS1+	Differential TMDS Data 1+
5	TMDS1_SHLD	TMDS Data1 Shield
6	TMDS1-	Differential TMDS Data 1-
7	TMDS0+	Differential TMDS Data 0+
8	TMDS0_SHLD	TMDS Data0 Shield
9	TMDS0-	Differential TMDS Data 0-
10	TMDSCLK-	Differential TMDS Clock-
11	TMDSCLK_SHLD	TMDS Clock Shield
12	TMDSCLK+	Differential TMDS Clock+
13	RSV	Reserved
14	RSV	Reserved
15	SCL	DDC EDID data clock
16	SDA	DDC EDID data
17	DDC/CEC GND	Ground
18	+5V	+5V / 500mA
19	HPD	HotPlug Detect



1.1

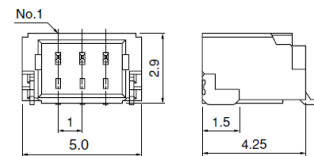
CN6 LVDS Input

Pin	Signal	Description	Pin	Signal	Description
1	TXA0-	LVDS data 1st pixel	16	TXB1+	LVDS data 2nd pixel
2	TXA0+	LVDS data 1st pixel	17	GND	Ground
3	TXA1-	LVDS data 1st pixel	18	TXB2-	LVDS data 2nd pixel
4	TXA1+	LVDS data 1st pixel	19	TXB2+	LVDS data 2nd pixel
5	TXA2-	LVDS data 1st pixel	20	TXBCL-	LVDS clock 2nd pixel
6	TXA2+	LVDS data 1st pixel	21	TXBCL+	LVDS clock 2nd pixel
7	GND	Ground	22	TXB3-	LVDS data 2nd pixel
8	TXACL-	LVDS clock 1st pixel	23	TXB3+	LVDS data 2nd pixel
9	TXACL+	LVDS clock 1st pixel	24	GND	Ground
10	TXA3-	LVDS data 1st pixel	25	NC	Not connected
11	TXA3+	LVDS data 1st pixel	26	NC	Not connected
12	TXVB0-	LVDS data 2nd pixel	27	NC	Not connected
13	TXVB0+	LVDS data 2nd pixel	28	VCC	Power supply Input +5V
14	GND	Ground	29		
15	TXB1-	LVDS data 2nd pixel	30		



CN8 Audio Output

Pin	Signal	Description
1	AOUTL	Audio out left
2	GND	Ground
3	AOUTR	Audio out right

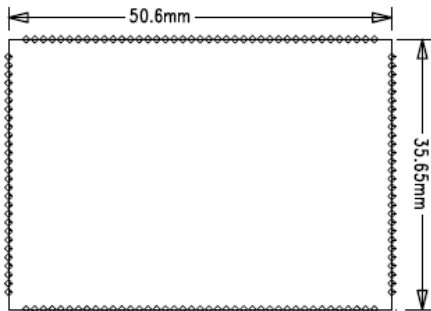


Connector Overview

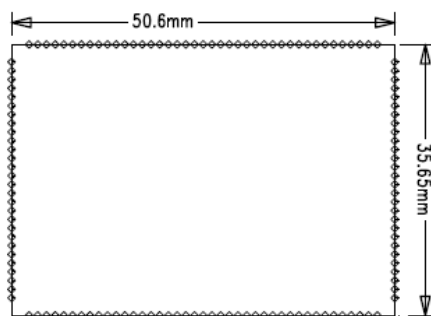
CN	Description	Type	Manufacturer
CN6	LVDS Input	FI-X30S-HF	JAE
CN7	HDMI Input	e.g. 685119134923	Würth
CN8	Audio Output	SM03B-SRSS-TB	JST
CN9	Power supply	S2B-PH-SM4-TB	JST
CN10	Power supply	53261-0271	Molex

5 Outline Dimension

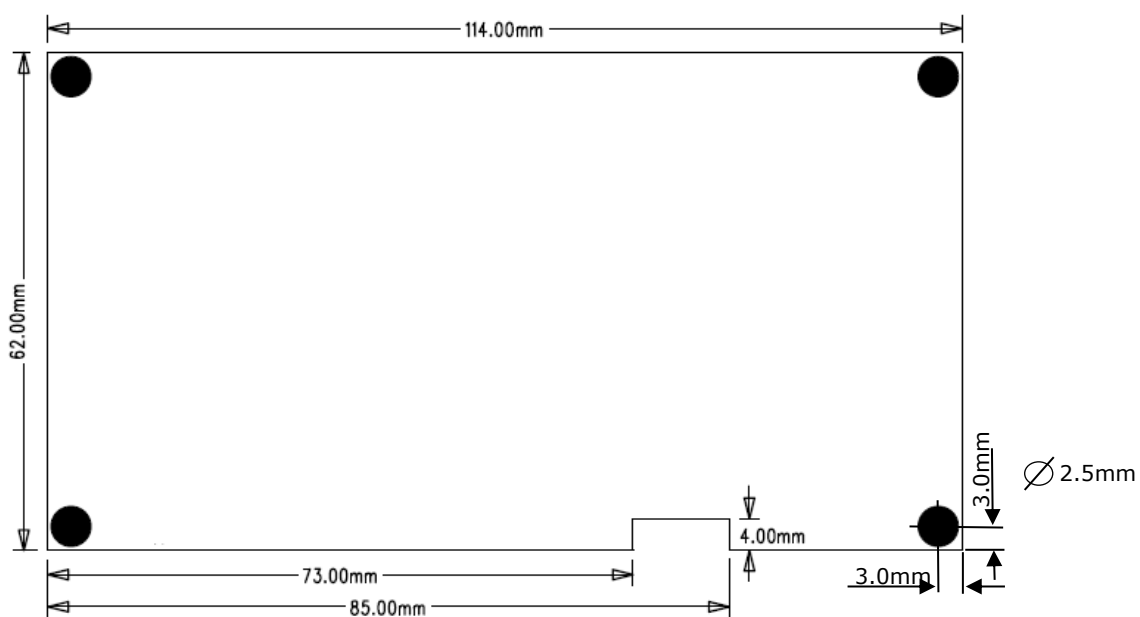
HDMI-to MIPI-DSI-Module



LVDS-to MIPI-DSI-Module

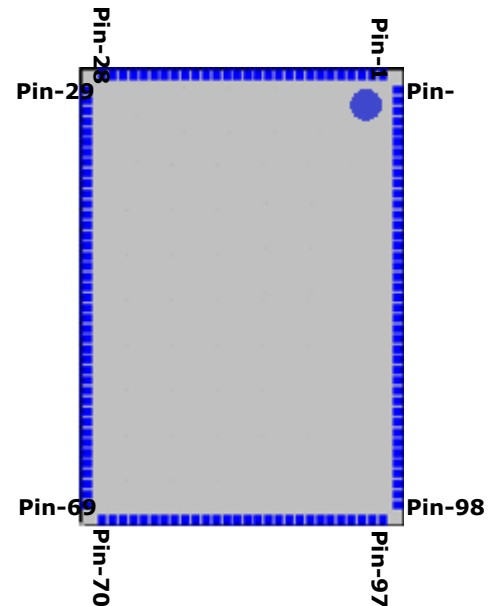


BaseBoard B-I



Appendix: BM – Bridge-Module Pin Assignment

Pin	Symbol	Description
1	GND	Ground
2	TMDS_XC-	TMDS-Clock-
3	TMDS_XC+	TMDS-Clock+
4	GND	Ground
5	TMDS_X0-	TMDS Data0-
6	TMDS_X0+	TMDS Data0+
7	GND	Ground
8	TMDS_X1-	TMDS Data1-
9	TMDS_X1+	TMDS Data1+
10	GND	Ground
11	TMDS_X2-	TMDS Data2-
12	TMDS_X2+	TMDS Data2+
13	GND	Ground
14	DP_AUX-	DisplayPort Auxiliary-
15	DP_AUX+	DisplayPort Auxiliary-
16	GND	Ground
17	DP_L3-	DisplayPort Lane3-
18	DP_L3+	DisplayPort Lane3+
19	GND	Ground
20	DP_L2-	DisplayPort Lane3-
21	DP_L2+	DisplayPort Lane3+
22	GND	Ground
23	DP_L1-	DisplayPort Lane3-
24	DP_L1+	DisplayPort Lane3+
25	GND	Ground
26	DP_L0-	DisplayPort Lane3-
27	DP_L0+	DisplayPort Lane3+
28	GND	Ground



Pin	Symbol	Description
29	DP_HPD	DP Hot-Plug-Detect
30	GND	Ground
31	LVDS_A0-	LVDS Channel-A Lane0-
32	LVDS_A0+	LVDS Channel-A Lane0+
33	GND	Ground
34	LVDS_A1-	LVDS Channel-A Lane1-
35	LVDS_A1+	LVDS Channel-A Lane1+
36	GND	Ground
37	LVDS_A2-	LVDS Channel-A Lane2-
38	LVDS_A2+	LVDS Channel-A Lane2+
39	GND	Ground
40	LVDS_CLK-	LVDS Channel-A Clock-
41	LVDS_CLK+	LVDS Channel-A Clock+

42	GND	Ground
43	LVDS_A3-	LVDS Channel-A Lane3-
44	LVDS_A3+	LVDS Channel-A Lane3+
45	GND	Ground
46	LVDS_B0-	LVDS Channel-B Lane0-
47	LVDS_B0+	LVDS Channel-B Lane0+
48	GND	Ground
49	LVDS_B1-	LVDS Channel-B Lane1-
50	LVDS_B1+	LVDS Channel-B Lane1+
51	GND	Ground
52	LVDS_B2-	LVDS Channel-B Lane2-
53	LVDS_B2+	LVDS Channel-B Lane2+
54	GND	Ground
55	LVDS_CLK-	LVDS Channel-B Clock-
56	LVDS_CLK+	LVDS Channel-B Clock+
57	GND	Ground
58	LVDS_B3-	LVDS Channel-B Lane3-
59	LVDS_B3+	LVDS Channel-B Lane3+
60	GND	Ground
61	UART_TXD	Serial-Port Transmit
62	UART_RX	Serial-Port Receive
62	NC	Not Connected
63	NC	Not Connected
64	NC	Not Connected
65	NC	Not Connected
66	NC	Not Connected
67	NC	Not Connected
68	NC	Not Connected
69	NC	Not Connected

Pin	Symbol	Description
70	GND	Ground
71	MIPI_A0-	MIPI Lane0-
72	MIPI_A0+	MIPI Lane0+
73	GND	Ground
74	MIPI_A1-	MIPI Lane1-
75	MIPI_A1+	MIPI Lane1+
76	GND	Ground
77	MIPI_C-	MIPI Clock-
78	MIPI_C+	MIPI Clock+
79	GND	Ground
80	MIPI_A2-	MIPI Lane2-
81	MIPI_A2+	MIPI Lane2+
82	GND	Ground
83	MIPI_A3-	MIPI Lane3-
84	MIPI_A3+	MIPI Lane3+
85	GND	Ground
86	+5V	+5.0V PS Input
87	+3.3V	+3.3V PS Input
88	IIS_D0	Serial Audio Data-0

89	IIS_D1	Serial Audio Data-1
90	IIS_D2	Serial Audio Data-2
91	IIS_D3/SPDIF	Serial Audio Data-0/SPDIF
92	IIS_SCLK	Serial Audio Clock
93	IIS_WS	Ser. Audio Left/Right Clk.
94	IIS_MCLK	Serial Audio Master-Clk.
95	GND	Ground
96	RST_IN	Reset Input
97	RST_out	Reset Output
Pin	Symbol	Description
98	NC	Not connected
99	PWM_GPIO3	Brightness-Ctrl / GPIO-3
100	ENVCC/GPIO2	En. Display VCC/ GPIO-2
101	ENEBKL/GPIO1	En. Backlight / GPIO-1
102	DE	Display Enable Signal
103	VSYNC	Display V-Sync Signal
104	HSYNC	Display H-Sync Signal
105	GND	Ground
106	CLK	Display Clock
107	GND	Ground
108	B7	Blue-7 / MSB
109	B6	Blue-6
110	B5	Blue-5
111	B4	Blue-4
112	B3	Blue-3
113	B2	Blue-2
114	B1	Blue-1
115	B0	Blue-0 / LSB
116	GND	Ground
117	G7	Green-7 / MSB
118	G6	Green-6
119	G5	Green-5
120	G4	Green-4
121	G3	Green-3
122	G2	Green-2
123	G1	Green-1
124	G0	Green-0 / LSB
125	GND	Ground
126	R7	Red-7 / MSB
127	R6	Red-6
128	R%	Red-5
129	R4	Red-4
130	R3	Red-3
131	R2	Red-2
132	R1	Red-1
133	R0	Red-0 / LSB
134	GND	Ground
135	CEC	Consumer electr. Ctrl.
136	DDC-SCL	DDC Clock
137	DDC-SDA	DDC Data
138	HPD_HDMI	HDMI Hot-Plug-Detect

Appendix: BM HDMI-to-MIPI-DSI

Pin Assignment and function of the HDMI-to-MIPI-DSI BridgeModule

Pin	Symbol	Description	Application
1	GND	Ground	Ground
2	TMDS_XC-	TMDS-Clock-	HDMI-Input
3	TMDS_XC+	TMDS-Clock+	HDMI-Input
4	GND	Ground	Ground
5	TMDS_X0-	TMDS Data0-	HDMI-Input
6	TMDS_X0+	TMDS Data0+	HDMI-Input
7	GND	Ground	Ground
8	TMDS_X1-	TMDS Data1-	HDMI-Input
9	TMDS_X1+	TMDS Data1+	HDMI-Input
10	GND	Ground	Ground
11	TMDS_X2-	TMDS Data2-	HDMI-Input
12	TMDS_X2+	TMDS Data2+	HDMI-Input
13	GND	Ground	Ground
14	DP_AUX-	DisplayPort Auxiliary-	
15	DP_AUX+	DisplayPort Auxiliary-	
16	GND	Ground	Ground
17	DP_L3-	DisplayPort Lane3-	
18	DP_L3+	DisplayPort Lane3+	
19	GND	Ground	Ground
20	DP_L2-	DisplayPort Lane3-	
21	DP_L2+	DisplayPort Lane3+	
22	GND	Ground	Ground
23	DP_L1-	DisplayPort Lane3-	
24	DP_L1+	DisplayPort Lane3+	
25	GND	Ground	Ground
26	DP_L0-	DisplayPort Lane3-	
27	DP_L0+	DisplayPort Lane3+	
28	GND	Ground	Ground

Pin	Symbol	Description	Application
29	DP_HPD	DP Hot-Plug-Detect	
30	GND	Ground	Ground
31	LVDS_A0-	LVDS Channel-A Lane0-	
32	LVDS_A0+	LVDS Channel-A Lane0+	
33	GND	Ground	Ground
34	LVDS_A1-	LVDS Channel-A Lane1-	
35	LVDS_A1+	LVDS Channel-A Lane1+	
36	GND	Ground	Ground
37	LVDS_A2-	LVDS Channel-A Lane2-	
38	LVDS_A2+	LVDS Channel-A Lane2+	
39	GND	Ground	Ground
40	LVDS_CLK-	LVDS Channel-A Clock-	
41	LVDS_CLK+	LVDS Channel-A Clock+	
42	GND	Ground	Ground

43	LVDS_A3-	LVDS Channel-A Lane3-	
44	LVDS_A3+	LVDS Channel-A Lane3+	
45	GND	Ground	Ground
46	LVDS_B0-	LVDS Channel-B Lane0-	
47	LVDS_B0+	LVDS Channel-B Lane0+	
48	GND	Ground	Ground
49	LVDS_B1-	LVDS Channel-B Lane1-	
50	LVDS_B1+	LVDS Channel-B Lane1+	
51	GND	Ground	Ground
52	LVDS_B2-	LVDS Channel-B Lane2-	
53	LVDS_B2+	LVDS Channel-B Lane2+	
54	GND	Ground	Ground
55	LVDS_CLK-	LVDS Channel-B Clock-	
56	LVDS_CLK+	LVDS Channel-B Clock+	
57	GND	Ground	Ground
58	LVDS_B3-	LVDS Channel-B Lane3-	
59	LVDS_B3+	LVDS Channel-B Lane3+	
60	GND	Ground	Ground
61	UART_TXD	Serial-Port Transmit	
62	UART_RX	Serial-Port Receive	
62	NC	Not Connected	
63	NC	Not Connected	
64	NC	Not Connected	
65	NC	Not Connected	
66	NC	Not Connected	
67	NC	Not Connected	
68	NC	Not Connected	
69	NC	Not Connected	

Pin	Symbol	Description	Application
70	GND	Ground	Ground
71	MIPI_A0-	MIPI Lane0-	MIPI-DSI Output
72	MIPI_A0+	MIPI Lane0+	MIPI-DSI Output
73	GND	Ground	Ground
74	MIPI_A1-	MIPI Lane1-	MIPI-DSI Output
75	MIPI_A1+	MIPI Lane1+	MIPI-DSI Output
76	GND	Ground	Ground
77	MIPI_C-	MIPI Clock-	MIPI-DSI Output
78	MIPI_C+	MIPI Clock+	MIPI-DSI Output
79	GND	Ground	Ground
80	MIPI_A2-	MIPI Lane2-	MIPI-DSI Output
81	MIPI_A2+	MIPI Lane2+	MIPI-DSI Output
82	GND	Ground	Ground
83	MIPI_A3-	MIPI Lane3-	MIPI-DSI Output
84	MIPI_A3+	MIPI Lane3+	MIPI-DSI Output
85	GND	Ground	Ground
86	+5V	+5.0V PS Input	Power Supply
87	+3.3V	+3.3V PS Input	
88	IIS_D0	Serial Audio Data-0	Audio Output
89	IIS_D1	Serial Audio Data-1	

90	IIS_D2	Serial Audio Data-2	
91	IIS_D3/SPDIF	Serial Audio Data-0/SPDIF	
92	IIS_SCLK	Serial Audio Clock	Audio Output
93	IIS_WS	Ser. Audio Left/Right Clk.	Audio Output
94	IIS_MCLK	Serial Audio Master-Clk.	Audio Output
95	GND	Ground	Ground
96	RST_IN	Reset Input	
97	RST_out	Reset Output	
Pin	Symbol	Description	Application
98	NC	Not connected	
99	PWM_GPIO3	Brightness-Ctrl / GPIO-3	
100	ENVCC/GPIO2	En. Display VCC/ GPIO-2	
101	ENEBKL/GPIO1	En. Backlight / GPIO-1	
102	DE	Display Enable Signal	
103	VSYNC	Display V-Sync Signal	
104	HSYNC	Display H-Sync Signal	
105	GND	Ground	Ground
106	CLK	Display Clock	
107	GND	Ground	Ground
108	B7	Blue-7 / MSB	
109	B6	Blue-6	
110	B5	Blue-5	
111	B4	Blue-4	
112	B3	Blue-3	
113	B2	Blue-2	
114	B1	Blue-1	
115	B0	Blue-0 / LSB	
116	GND	Ground	Ground
117	G7	Green-7 / MSB	
118	G6	Green-6	
119	G5	Green-5	
120	G4	Green-4	
121	G3	Green-3	
122	G2	Green-2	
123	G1	Green-1	
124	G0	Green-0 / LSB	
125	GND	Ground	Ground
126	R7	Red-7 / MSB	
127	R6	Red-6	
128	R%	Red-5	
129	R4	Red-4	
130	R3	Red-3	
131	R2	Red-2	
132	R1	Red-1	
133	R0	Red-0 / LSB	
134	GND	Ground	Ground
135	CEC	Consumer electr. Ctrl.	
136	DDC-SCL	DDC Clock	HDMI-Input
137	DDC-SDA	DDC Data	HDMI-Input
138	HPD_HDMI	HDMI Hot-Plug-Detect	HDMI-Input

Appendix: BM LVDS-to-MIPI-DSI

Pin Assignment and function of the LVDS-to-MIPI-DSI BridgeModule

Pin	Symbol	Description	Application
1	GND	Ground	Ground
2	TMDS_XC-	TMDS-Clock-	
3	TMDS_XC+	TMDS-Clock+	
4	GND	Ground	Ground
5	TMDS_X0-	TMDS Data0-	
6	TMDS_X0+	TMDS Data0+	
7	GND	Ground	Ground
8	TMDS_X1-	TMDS Data1-	
9	TMDS_X1+	TMDS Data1+	
10	GND	Ground	Ground
11	TMDS_X2-	TMDS Data2-	
12	TMDS_X2+	TMDS Data2+	
13	GND	Ground	Ground
14	DP_AUX-	DisplayPort Auxiliary-	
15	DP_AUX+	DisplayPort Auxiliary-	
16	GND	Ground	Ground
17	DP_L3-	DisplayPort Lane3-	
18	DP_L3+	DisplayPort Lane3+	
19	GND	Ground	Ground
20	DP_L2-	DisplayPort Lane3-	
21	DP_L2+	DisplayPort Lane3+	
22	GND	Ground	Ground
23	DP_L1-	DisplayPort Lane3-	
24	DP_L1+	DisplayPort Lane3+	
25	GND	Ground	Ground
26	DP_L0-	DisplayPort Lane3-	
27	DP_L0+	DisplayPort Lane3+	
28	GND	Ground	Ground

Pin	Symbol	Description	Application
29	DP_HPD	DP Hot-Plug-Detect	
30	GND	Ground	Ground
31	LVDS_A0-	LVDS Channel-A Lane0-	LVDS Input
32	LVDS_A0+	LVDS Channel-A Lane0+	LVDS Input
33	GND	Ground	Ground
34	LVDS_A1-	LVDS Channel-A Lane1-	LVDS Input
35	LVDS_A1+	LVDS Channel-A Lane1+	LVDS Input
36	GND	Ground	Ground
37	LVDS_A2-	LVDS Channel-A Lane2-	LVDS Input
38	LVDS_A2+	LVDS Channel-A Lane2+	LVDS Input
39	GND	Ground	Ground
40	LVDS_CLK-	LVDS Channel-A Clock-	LVDS Input
41	LVDS_CLK+	LVDS Channel-A Clock+	LVDS Input
42	GND	Ground	Ground

43	LVDS_A3-	LVDS Channel-A Lane3-	LVDS Input
44	LVDS_A3+	LVDS Channel-A Lane3+	LVDS Input
45	GND	Ground	Ground
46	LVDS_B0-	LVDS Channel-B Lane0-	LVDS Input
47	LVDS_B0+	LVDS Channel-B Lane0+	LVDS Input
48	GND	Ground	Ground
49	LVDS_B1-	LVDS Channel-B Lane1-	LVDS Input
50	LVDS_B1+	LVDS Channel-B Lane1+	LVDS Input
51	GND	Ground	Ground
52	LVDS_B2-	LVDS Channel-B Lane2-	LVDS Input
53	LVDS_B2+	LVDS Channel-B Lane2+	LVDS Input
54	GND	Ground	Ground
55	LVDS_CLK-	LVDS Channel-B Clock-	LVDS Input
56	LVDS_CLK+	LVDS Channel-B Clock+	LVDS Input
57	GND	Ground	Ground
58	LVDS_B3-	LVDS Channel-B Lane3-	LVDS Input
59	LVDS_B3+	LVDS Channel-B Lane3+	LVDS Input
60	GND	Ground	Ground
61	UART_TXD	Serial-Port Transmit	
62	UART_RX	Serial-Port Receive	
62	NC	Not Connected	
63	NC	Not Connected	
64	NC	Not Connected	
65	NC	Not Connected	
66	NC	Not Connected	
67	NC	Not Connected	
68	NC	Not Connected	
69	NC	Not Connected	

Pin	Symbol	Description	Application
70	GND	Ground	Ground
71	MIPI_A0-	MIPI Lane0-	MIPI-DSI Output
72	MIPI_A0+	MIPI Lane0+	MIPI-DSI Output
73	GND	Ground	Ground
74	MIPI_A1-	MIPI Lane1-	MIPI-DSI Output
75	MIPI_A1+	MIPI Lane1+	MIPI-DSI Output
76	GND	Ground	Ground
77	MIPI_C-	MIPI Clock-	MIPI-DSI Output
78	MIPI_C+	MIPI Clock+	MIPI-DSI Output
79	GND	Ground	Ground
80	MIPI_A2-	MIPI Lane2-	MIPI-DSI Output
81	MIPI_A2+	MIPI Lane2+	MIPI-DSI Output
82	GND	Ground	Ground
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113	B2	Blue-2	
114	B1	Blue-1	
115	B0	Blue-0 / LSB	
116	GND	Ground	Ground
117	G7	Green-7 / MSB	
118	G6	Green-6	
119	G5	Green-5	
120	G4	Green-4	
121	G3	Green-3	
122	G2	Green-2	
123	G1	Green-1	
124	G0	Green-0 / LSB	
125	GND	Ground	Ground
126	R7	Red-7 / MSB	
127	R6	Red-6	
128	R%	Red-5	
129	R4	Red-4	
130	R3	Red-3	
131	R2	Red-2	
132	R1	Red-1	
133	R0	Red-0 / LSB	
134	GND	Ground	Ground
135	CEC	Consumer electr. Ctrl.	
136	DDC-SCL	DDC Clock	
137	DDC-SDA	DDC Data	
138	HPD_HDMI	HDMI Hot-Plug-Detect	

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, Great Britain and the USA. For more information please contact:

Headquarters

Germany



FORTEC Elektronik AG
Lechwiesenstr. 9
86899 Landsberg am Lech

Phone: +49 8191 91172-0
E-Mail: sales@fortecag.de
Internet: www.fortecag.de

Fortec Group Members

Austria



FORTEC Elektronik AG
Office Vienna

Nuschinggasse 12
1230 Wien

Phone: +43 1 8673492-0
E-Mail: office@fortec.at
Internet: www.fortec.at

Germany



Distec GmbH

Augsburger Str. 2b
82110 Germering

Phone: +49 89 894363-0
E-Mail: info@distec.de
Internet: www.distec.de

Switzerland



ALTRAC AG

Bahnhofstraße 3
5436 Würenlos

Phone: +41 44 7446111
E-Mail: info@altrac.ch
Internet: www.altrac.ch

Great Britain



Display Technology Ltd.

5 The Oaks Business Village
Revenge Road, Lordswood
Chatham, Kent, ME5 8LF

Phone: +44 1634 672755
E-Mail: info@displaytechnology.co.uk
Internet: www.displaytechnology.co.uk

USA



Apollo Display Technologies, Corp.

87 Raynor Avenue,
Unit 1 Ronkonkoma,
NY 11779

Phone: +1 631 5804360
E-Mail: info@apolloDisplays.com
Internet: www.apolloDisplays.com