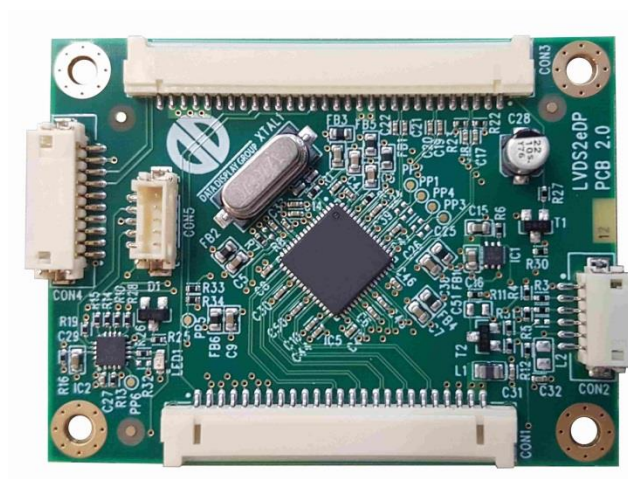


Datasheet

LVDS2eDP

LVDS to eDP Converter

ZU-09-034 LVDS2EDP-03 INTERFACE BOARD (3,3V)
ZU-09-036 LVDS2EDP-04 INTERFACE BOARD (5V/12V)



Version 2.3

18.05.2018

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Revision History

Date	Rev.No.	Description	Page
24.06.2014	1.0	Initial version	All
16.07.2014	1.1	Reformat and add Connectors pinning	All
25.07.2014	1.1	Added Board Picture, removed Preliminary notice	All
07.08.2014	1.1	Clarified Odd, Even Pixel	7
12.11.2014	1.2	PCB 1.1 changes are implemented Added IPC usage	All
14.11.2014	1.3	Corrected pinout description of CON1	7
26.01.2014	1.4	Removed 1 lane	5
19.11.2015	1.5	Added power consumption	9
04.12.2015	1.6	Added Cables section	4, 9, 10
19.01.2016	1.7	Corrected CON3 HPD pin	8
16.02.2016	1.8	Corrected connector type of CON4 and CON5	8, 9
15.03.2016	1.9	Document completely revised	All
14.06.2016	1.10	Company logo update Operating Temperature Range updated	All 16
12.07.2016	1.11	Add new Part Number ZU-09-032_A1 and ZU-09-029_A2 Add Ordering Information	1, 18
22.11.2016	1.12	Added panels NL192108AC18-01D and LP125WF2-SPB2 Added cable and FW information to HW options	8 4, 5
06.07.2017	1.13	Mechanical Dimensions updated News and Updates removed	17 18
18.10.2017	2.0	Datasheet completely revised due to new HW revision 2.0	All
28.11.2017	2.1	Corrected pin-out of CON1, added LED error codes	9, 11
14.02.2018	2.2	Replaced obsolete ArtistaMedia-II by ArtistaMedia-III	12
18.05.2018	2.3	Added note to CON4	11

1 Description

LVDS2eDP is an interface board that converts LVDS data to embedded DisplayPort. It is used when a flat screen panel with eDP input has to be connected to a source (e.g. an industrial PC) which provides only an LVDS output signal.

1.1 Features

- Single and dual link LVDS input
- Supports 6bit and 8bit color depth
- Open LDI / JEIDA and VESA LVDS data mapping
- LVDS input clock rates up to 165MHz for Single Link and up to 135MHz for Dual Link
- Input and output resolution up to 1920x1200@60Hz
- eDP output compliant with DisplayPort 1.1a
- Supports two lanes eDP output with HBR (2.7Gpbs) and RBR (1.62Gpbs)
- Can be connected to our standard Prisma and Artista controller boards and standard IPCs
- HDCP is not supported
- Panel voltage comes directly from the input source and is not regulated on the board
- Backlight voltage comes directly from the input source and is not regulated on the board

1.2 Overview

LVDS2eDP is available in the following two HW versions:

ZU-09-034 LVDS2EDP-03 INTERFACE BOARD (3,3V)

This interface supports TFT panels which need 3.3V digital supply voltage.

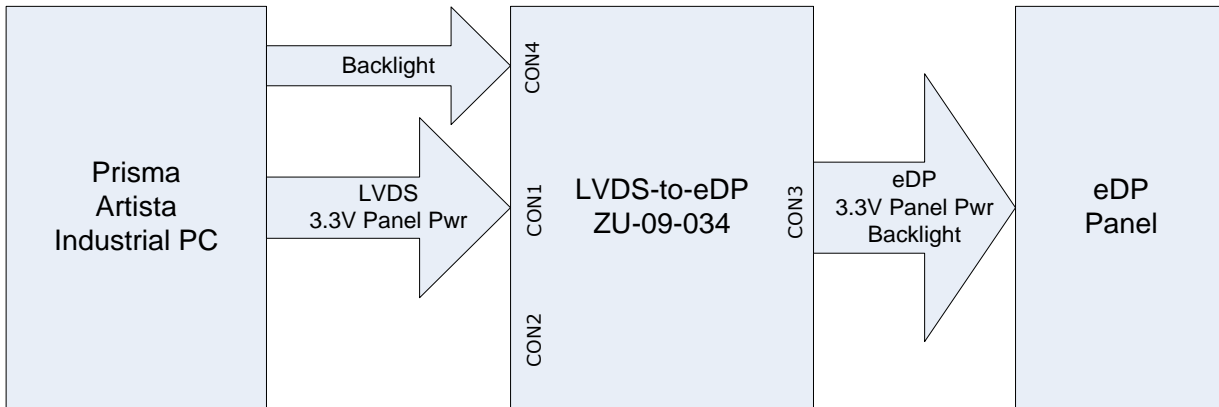
ZU-09-036 LVDS2EDP-04 INTERFACE BOARD (5V/12V)

This interface supports TFT panels which need 5V or 12V digital supply voltage.

Both HW versions have to be loaded with a FW that is configured according to the output format of the LVDS source and the used panel (single or dual link LVDS, LVDS data mapping, color depth). See section 10 for ordering codes of configured LVDS2eDP interfaces.

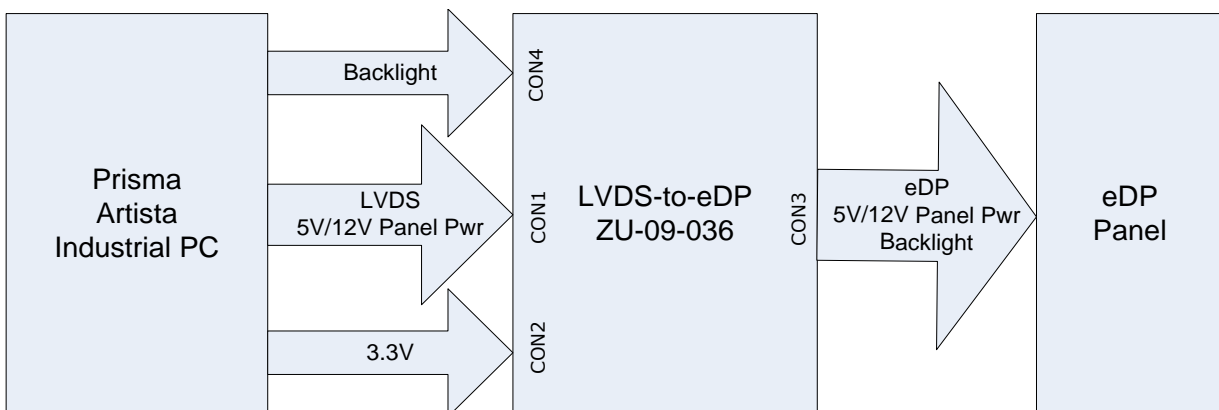
2 Cabling

2.1 3.3V Panel Power



Use the 3.3V version of the LVDS2eDP interface (ZU-09-034) if your panel power is 3.3V. In this case the LVDS2eDP interface is supplied directly by the 3.3V panel power via CON1. Backlight power and brightness control signals from the source are connected to CON4, these signals go directly to the output connector CON3. A single cable connects CON3 to the eDP input of the TFT panel. Do not connect any cable to CON2. See section 6 for ordering numbers of these cables.

2.2 5V and 12V Panel Power



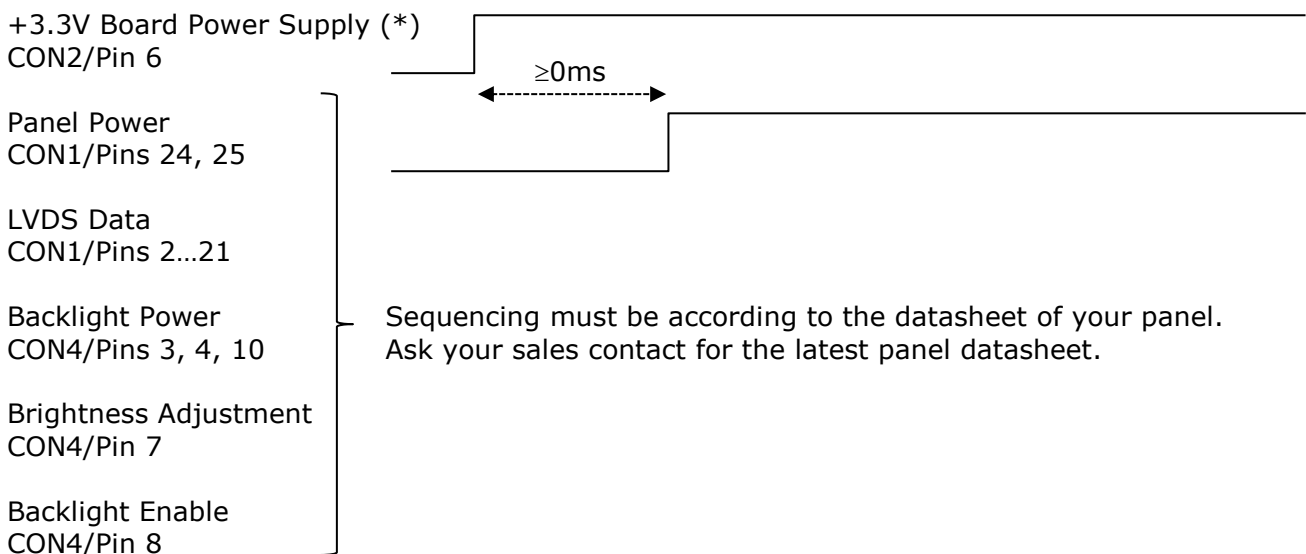
Use the 5V/12V version of the LVDS2eDP interface (ZU-09-036) if the panel power is 5V or 12V. In this case an additional 3.3V power supply must be connected to CON2. All other cables are equal to section 2.1.

3 Operating Conditions

To ensure a stable operation of the LVDS2eDP interface the user must ensure that the power and control signals to the inputs of the interface comply with the following requirements.

3.1 Power Sequencing

It is important to switch on the power supplies and data signals in a defined sequence. The required sequence of the LVDS2eDP interface is shown in the following diagram. Please note that additionally the sequencing specification from the panel datasheet must be met.



(*) Only needed for ZU-09-036 (5V or 12V panel power)

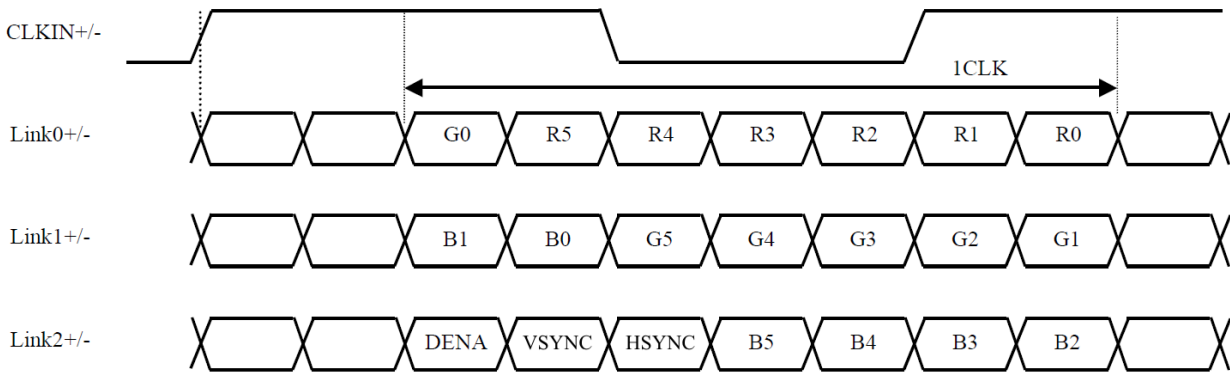
3.2 LVDS Input Timing

The LVDS timing (number of active and total pixels, back- and front porch, sync width and sync polarity) has to meet the timing specified in the panel datasheet. The LVDS2eDP interface outputs the exact timing that is captured on its LVDS input.

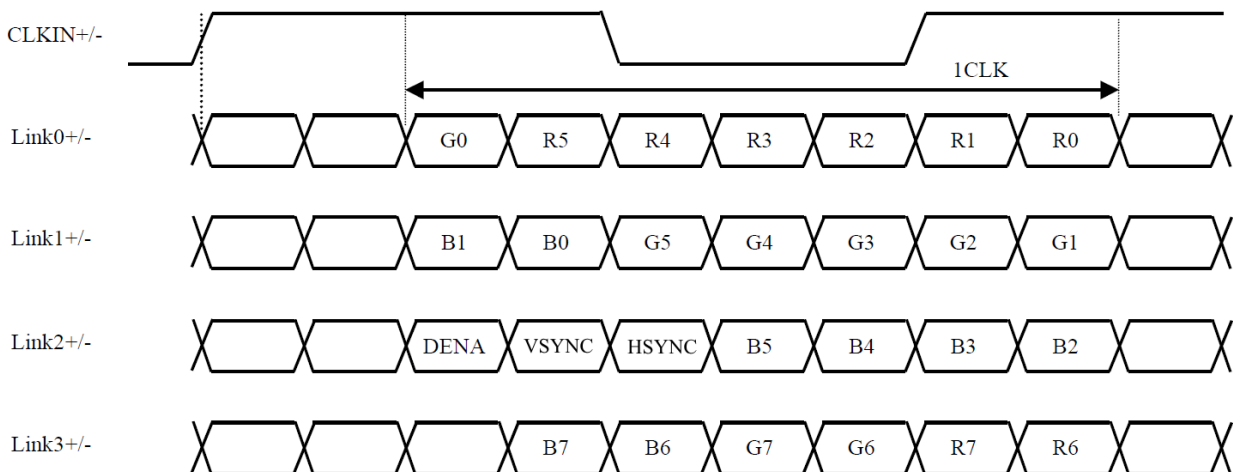
3.3 LVDS Data Mapping

The input format of the LVDS data on CON1 has to comply with the following data mappings. See sec. 10 for the ordering code of the required mapping.

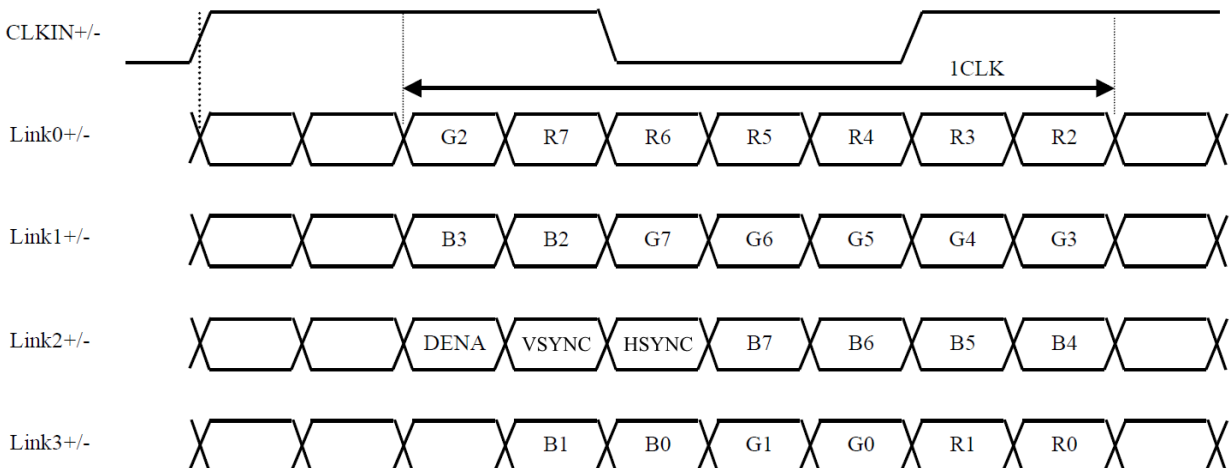
18 Bit LVDS Input Data:



24 Bit LVDS Input Data with VESA Mapping:



24 Bit LVDS Input Data with JEIDA Mapping:



4 Connectors

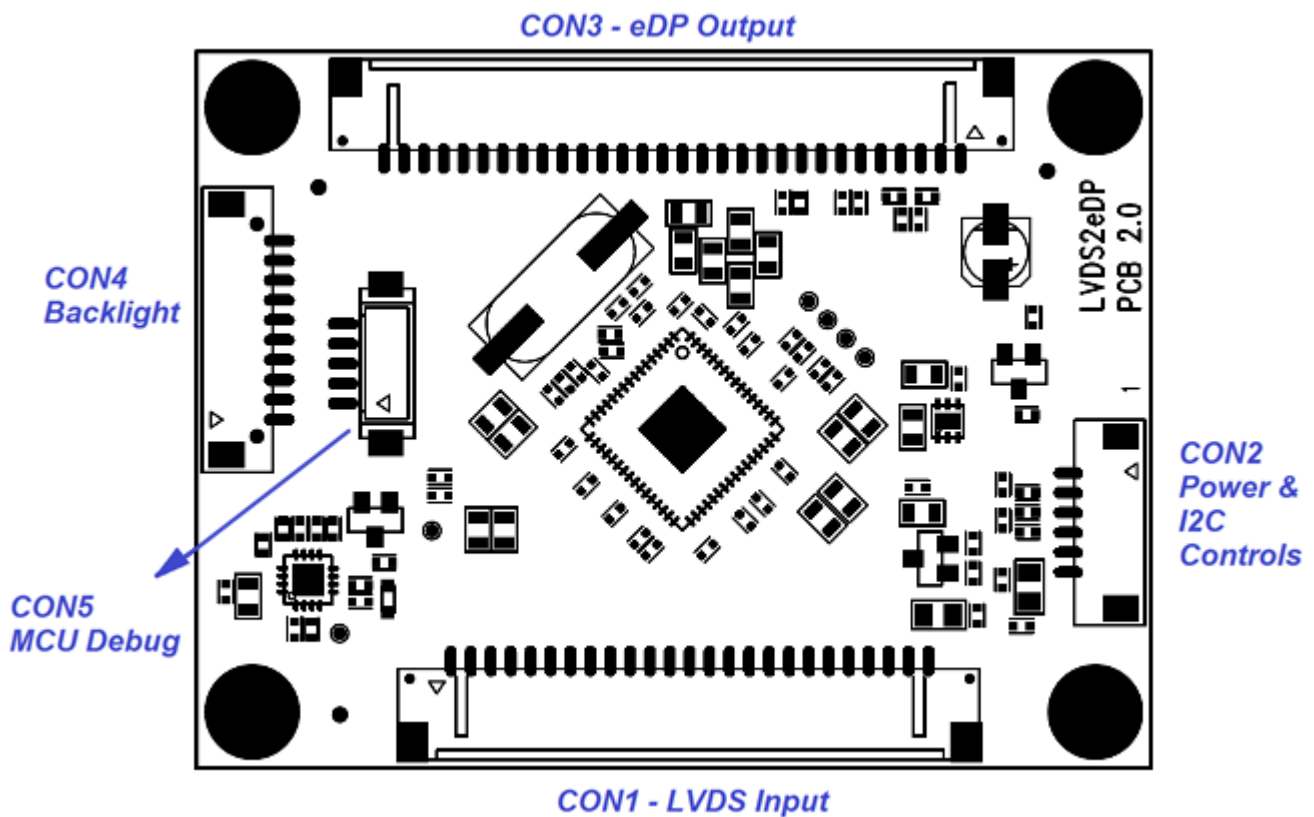


Figure 1: Connectors overview

Connector	Usage	Manufacturer Part Number Hirose
CON1	LVDS & Panel Power Input	DF14-25P-1.25H
CON2	I2C & Board Power Supply Input	DF13-6P-1.25H
CON3	eDP Output	DF14-30P-1.25H
CON4	Backlight Power & Control Input	DF13-10P-1.25H
CON5	MCU Debug	DF13-5P-1.25V

4.1 CON1 – LVDS & Panel Power Input

Manufacturer : Hirose
Type : DF14-25P-1.25H

Pin	Signal	Description
1	BKLT_EN	Backlight Enable
2	RXB0-	LVDS Input Even Pixel Pair0 -
3	RXB0+	LVDS Input Even Pixel Pair0 +
4	RXB1-	LVDS Input Even Pixel Pair1 -
5	RXB1+	LVDS Input Even Pixel Pair1 +
6	RXB2-	LVDS Input Even Pixel Pair2 -
7	RXB2+	LVDS Input Even Pixel Pair2 +
8	nc	Not connected
9	nc	Not connected
10	RXB3-	LVDS Input Even Pixel Pair3 -
11	RXB3+	LVDS Input Even Pixel Pair3 +
12	RXA0-	LVDS Input Odd Pixel Pair0 -
13	RXA0+	LVDS Input Odd Pixel Pair0 +
14	RXA1-	LVDS Input Odd Pixel Pair1 -
15	RXA1+	LVDS Input Odd Pixel Pair1 +
16	RXA2-	LVDS Input Odd Pixel Pair2 -
17	RXA2+	LVDS Input Odd Pixel Pair2 +
18	RXACLK-	LVDS Input Odd Pixel Clock -
19	RXACLK+	LVDS Input Odd Pixel Clock +
20	RXA3-	LVDS Input Odd Pixel Pair3 -
21	RXA3+	LVDS Input Odd Pixel Pair3 +
22	GND	Ground
23	GND	Ground
24	SVCC	Panel Power (Note 2)
25	SVCC	Panel Power (Note 2)

Notes:

- 1) Odd pixel is the first pixel.
- 2) If you use ZU-09-034 only 3.3V panel power is allowed. See sec. 2 for more details.

4.2 CON2 – I2C and external Power Supply

Use this connector only if your panel power is 5V or 12V.

Manufacturer : Hirose
Type : DF13-6P-1.25H

Pin	Signal	Description
1	GND	Ground
2	SDA	I ² C data (keep this pin unconnected)
3	SCL	I ² C clock (keep this pin unconnected)
4	RST	Optional Reset (keep this pin unconnected)
5	HPD#	Inverted Hot Plug Detect (keep this pin unconnected)
6	+3.3V Vin	+3.3V Board Power Supply (only for ZU-09-036)

4.3 CON3 – eDP Output

Manufacturer : Hirose
Type : DF14-30P-1.25H

Pin	Signal	Description
1	--	Not connected
2	GND	Ground
3	DPAUX+	eDP Aux Channel +
4	DPAUX-	eDP Aux Channel -
5	GND	Ground
6	DP0-	eDP Channel 0 -
7	DP0+	eDP Channel 0 +
8	GND	Ground
9	DP1-	eDP Channel 1 -
10	DP1+	eDP Channel 1 +
11	GND	Ground
12	SVCC	Panel Power Output (Note 1)
13	SVCC	Max. 1A (Note 3)
14	--	Not connected
15	GND	Ground
16	GND	Ground
17	HPD	Hot Plug Detect
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	BKLT_EN	Backlight Enable - Output (Note 2)
23	BRT_ADJ	Backlight Dimming - PWM Output (Note 2)
24	--	Not connected
25	--	Not connected
26	+12V_BKLT	+12V Backlight Power Output (Note 2)
27	+12V_BKLT	Max. 2A (Note 3)
28	+12V_BKLT	
29	+12V_BKLT	
30	--	Not connected

Notes:

- 1) Directly connected to SVCC of CON1
- 2) All backlight signals are directly connected to CON4
- 3) This is the max. allowed current of the LVDS2eDP interface. The max. allowed current of the connected input source (IPC) must be considered as well. The LVDS2eDP interface does not provide any current limitation circuitry or fuses.

4.4 CON4 – Backlight Input

Manufacturer : Hirose
Type : DF13-10P-1.25H

Pin	Signal	Description
1	GND	Ground
2	GND	Ground
3	+12V_BKLT	+12V Backlight Supply Input
4	+12V_BKLT	+12V Backlight Supply Input
5	--	Not connected
6	--	Not connected
7	BRT_ADJ	Backlight Dimming – PWM Input
8	BKLT_EN	Backlight Enable – Input
9	GND	Ground
10	+12V_BKLT	+12V Backlight Supply Input

Note:

CON4 can be left completely unconnected if the customer provides backlight power and backlight control signals directly to the panel.

4.5 CON5 – MCU Debug

This connector is for engineering and production purposes.

Manufacturer : Hirose
Type : DF13-5P-1.25V

Pin	Signal	Description
1	RESET	Programming Reset
2	SWD_DIO	Programming Data
3	PROG_3.3V	Programming Voltage
4	SWD_CLK	Programming Clock
5	GND	Ground

5 LED

The green LED on the board shows the status of the eDP chip.

LED permanently on: Everything is OK

- eDP panel connected (HPD status is "plugged")
- LVDS input stable

LED fast blinking (3Hz): Error

- eDP panel not connected (HPD status is "unplugged")
- On ZU-09-036 this can also mean that panel power is off

LED slowly blinking (0.5Hz): Error

- LVDS input unstable

LED very slowly blinking (0.1Hz): Error

- eDP chip is not initialized
- On ZU-09-034 this can mean that an external cable is detected on CON2

6 Cables

6.1 LVDS Cable (connects to CON1)

Driving Board	Prisma/Artista Connector	Connector Part Number	Cable Order Code
ArtistaMedia-III Artista-IoT VideoPoster-IV	CON13	DF14-25P-1.25H	KA-30-520
ArtistaNET-III	CON7		
Prisma-IIIA	CON4		
PrismaMediaECO	CN10		
PrismaCompactMedia	CON10	DF14-30P-1.25H	KA-30-877

6.2 Backlight Cable (connects to CON4)

Driving Board	Prisma/Artista Connector	Connector Part Number	Cable Order Code
ArtistaMedia-III Artista-IoT VideoPoster-IV	CON16	DF13-10P-1.25H	KA-30-521
ArtistaNET-III	CON14		
Prisma-IIIA	CON23		
PrismaMediaECO	CN13		
PrismaCompactMedia	CON13	DF13-10P-1.25H	KA-30-878

6.3 eDP Cable (connects to CON3)

eDP Panel (example)	eDP Connector	Cable Length	Cable Order Code
LP156WF6-SPB1 LP125WF2-SPB2 LP173WF4-SPF5	IPEX 30 Pins	100mm	KA-30-541
VVX12F045J00 VVX10F087J00	IPEX 30 Pins	100mm	KA-30-803
G156HAN01.0	IPEX 40 Pins	100mm	KA-30-754
NL192108AC18-01D NL192108AC13-02D	IPEX 40 Pins	100mm	KA-30-758
NL192108BC18-06F (Note 2)	IPEX 40 Pins	100mm	KA-30-859

Notes:

- 1) Other cables available upon request.
- 2) External LED converter needed (IN-54-010 with KA-25-024)

7 Electrical Requirements

7.1 Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Board Power Supply ZU-09-036	V_{IN}	3.1	3.3	3.6	V	CON2, Pin6
Board Power Supply ZU-09-034	V_{IN}	3.1	3.3	3.6	V	CON1, Pin24+25 See note 1 below
Supply Current (board only, without panel)	I_{IN}		350	400	mA	Processing video format: 1920x1080@60Hz

Notes:

1) This is the voltage range of the LVDS2eDP interface. The voltage range of the connected eDP panel must be considered as well. The input voltage on CON1 is directly connected to the panel, the LVDS2eDP interface does not provide any voltage regulation circuitry.

7.2 Absolute Maximum Ratings

Permanent damage to the device may occur if maximum values are exceeded.

Item	Symbol	Min.	Max.	Unit	Note
Board Power Supply	V_{IN}	-0.2	3.6	V	
Panel Voltage Input ZU-09-036	V_{PNL}	-0.2	13	V	CON1, Pin24+25 See note 1 below
Panel Voltage Input ZU-09-034	V_{PNL}	-0.2	3.6	V	CON1, Pin24+25 See note 1 below
Panel Current	I_{PNL}		1	A	See note 2 below
Backlight Voltage Input	V_{BKL}	-0.2	25	V	CON4, Pin 3+4+10 See note 1 below
Backlight Current	I_{BKL}		2	A	See note 2 below

Notes:

1) This is the max. allowed voltage of the LVDS2eDP interface. The max. allowed voltage of the connected eDP panel must be considered as well. The input voltage on CON1 is directly connected to the panel, the LVDS2eDP interface does not provide any voltage regulation circuitry.

2) This is the max. allowed current of the LVDS2eDP interface. The max. allowed current of the connected input source (IPC) must be considered as well. The LVDS2eDP interface does not provide any current limitation circuitry or fuses.

8 Thermal Ratings

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_{op}	-20	+80	$^{\circ}C$	
Storage Temperature	T_{st}	-35	+85	$^{\circ}C$	

9 Mechanical Dimensions

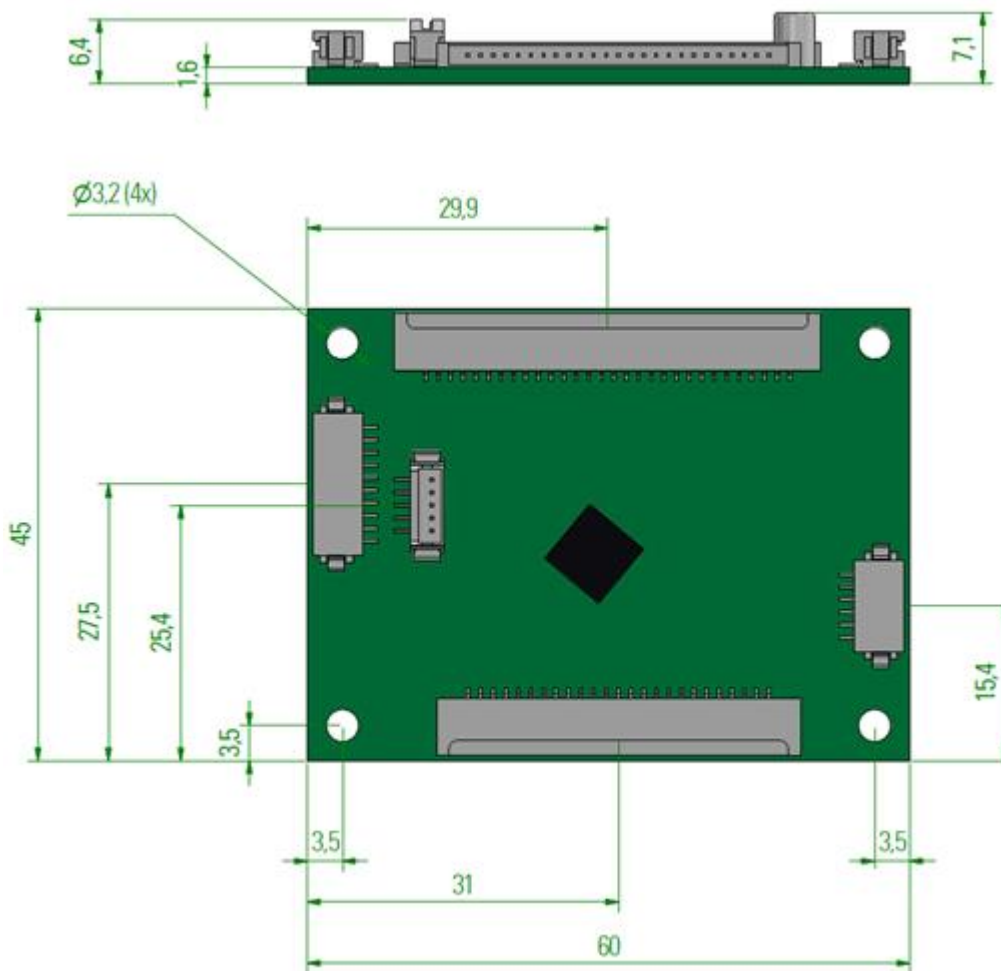


Figure 2: Dimensions

10 Ordering Information

It is important that the configuration of the LVDS2eDP interface matches with the data format of the LVDS source and the color depth of the panel, otherwise color mismatch or image distortion will occur.

Part Number HW only	Part Number incl. FW	Supported Panel Voltages	Color Depth	LVDS Input Mapping	LVDS Channels	Operating Temperature Range
ZU-09-034	DB-10-020	3.3V	18 Bits	JEIDA	Dual	-20°C to +80°C
	DB-10-021	3.3V	24 Bits	JEIDA	Dual	-20°C to +80°C
	DB-10-022	3.3V	24 Bits	VESA	Dual	-20°C to +80°C
ZU-09-036	*	5V, 12V	*	*	*	-20°C to +80°C

* Contact your sales representative for 5V and 12V panel support.

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